

COMPARISON OF MIL-STD-883
AND HI-REL "K" TEST PROGRAM

MIL-STD-883B, METHOD 5004.4, CLASS B	HI-REL "K" TEST
3.1.1 Internal Visual Method 2010.3 Test condition B	All Hi-Rel "K" devices receive 100% inspections prior to lid seal. These inspections together comprise criteria comparable to Mil-Std-883, method 2010.3, test condition B.
3.1.2 Stabilization Bake Method 1008.1 Test condition C 24 hours at 150°C	Same
3.1.3 Temperature Cycling Method 1010.2, Test condition C - 65°C to 150°C for 10 cycles, with 10 minutes dwell and 5 minutes maximum transfer time	Same
3.1.4 Constant Acceleration Method 2001.2, Test condition E. 30,000 G stress level	Not Done Unless Specified
3.1.5 Visual Inspection Visual inspection for catastrophic failures after screens	Same
3.1.6 Seal Method 1014.2 (a) Helium fine leak — Test condition A ₁ . Bomb condition 2 hours at 60 psig. Reject limit 5 x 10 ⁻⁹ torr (b) Fluorocarbon gross leak — Test condition C	Same
3.1.9 Interim (pre-burn-in) Electricals Per applicable device specification	Preburn-in test at 25°C. Must meet requirements of device data sheets.
3.1.10 Burn-in Test Method 1015.2 160 hours @ 125°C	Same
3.1.13 Interim (Post burn-in) electricals Per applicable device specification	Burn-in equipment isolate failures automatically to assure no harmful interaction.
3.1.15 Final Electrical Test (a) Static Tests (1) 25°C (2) Minimum and Maximum Operating Temperatures (b) Dynamic and Switching Tests at 25°C (c) Functional Tests at 25°C	Same
3.1.17 Qualification or Quality Conformance Inspection and Test Sample Selection	Not done unless defined using method 5005 as a guide.
3.1.18 External Visual Method 2009.2	Same
WESTERN DIGITAL RELIABILITY ENHANCEMENT OPTIONS	
100% Temperature Testing Level - 40° to + 85°C - 55° to + 125°C	Extended High Temperature Storage + 150°C for 24 hours standard, other time/temperature storage requirements available as required.
Thermal, Shock (Liquid to Liquid) Level 0° to + 100°C, 15 cycles - 55° to + 125°C - 65° to + 150°C	Dynamic Burn-In Per note previously supplied.

WESTERN DIGITAL
CORPORATION

FD1771-01 Floppy Disk Formatter/Controller

FD1771-01

FEATURES

- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- READ MODE
Single/Multiple Sector Write with Automatic Sector Search or Entire Track Read
Selectable 128 Byte or Variable Length Sector
- WRITE MODE
Single/Multiple Sector Write with Automatic Sector Search
Entire Track Write for Diskette Formatting
- PROGRAMMABLE CONTROLS
Selectable Track-to-Track Stepping Time
Selectable Head Settling and Head Engage Times
Selectable Three Phase or Step and Direction and Head Positioning Motor Controls
- SYSTEM COMPATIBILITY
Double Buffering of Data 8-Bit Bi-Directional Bus for Data, Control and Status
DMA or Programmed Data Transfers
All Inputs and Outputs are TTL Compatible

APPLICATIONS

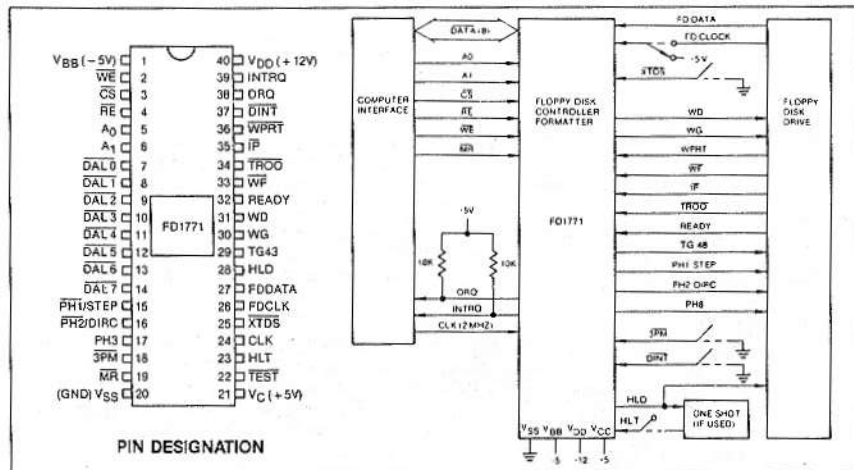
FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE
CONTROLLER/FORMATTER
NEW MINI-FLOPPY CONTROLLER

GENERAL DESCRIPTION

The FD1771 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface organization that accommodates the interface signals from most drive manufacturers. The FD1771 is compatible with the IBM 3740 data entry system format.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD1771 is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD1771 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The A and B suffixes are for ceramic and plastic packages, respectively.



FD1771 SYSTEM BLOCK DIAGRAM

PIN OUTS

Pin No.	Pin Name	Symbol	Function																				
1	Power Supplies	V _{BG} /NC	-5V																				
19	MASTER RESET	MR	A logic low on this input resets the device and loads "03" into the command register. The Not Ready (Status bit 7) is reset during MR ACTIVE. When MR is brought to a logic high, a Restore Command is executed, regardless of the state of the Ready signal from the drive.																				
20		V _{SS}	Ground																				
21		V _{CC}	+5V																				
40		V _{DD}	+12V																				
Computer Interface																							
2	WRITE ENABLE	WE	A logic low on this input gates data on the DAL into the selected register when CS is low.																				
3	CHIP SELECT	CS	A logic low on this input selects the chip and enables computer communication with the device.																				
4	READ ENABLE	RE	A logic low on this input controls the placement of data from a selected register on the DAL when CS is low.																				
5, 6	REGISTER SELECT LINES	A ₀ , A ₁	These inputs select the register to receive/transfer data on the DAL lines under RE and WE control: <table border="0" style="margin-left: 20px;"> <tr> <td>A₁</td> <td>A₀</td> <td>RE</td> <td>WE</td> </tr> <tr> <td>0</td> <td>0</td> <td>Status Register</td> <td>Command Register</td> </tr> <tr> <td>0</td> <td>1</td> <td>Track Register</td> <td>Track Register</td> </tr> <tr> <td>1</td> <td>0</td> <td>Sector Register</td> <td>Sector Register</td> </tr> <tr> <td>1</td> <td>1</td> <td>Data Register</td> <td>Data Register</td> </tr> </table>	A ₁	A ₀	RE	WE	0	0	Status Register	Command Register	0	1	Track Register	Track Register	1	0	Sector Register	Sector Register	1	1	Data Register	Data Register
A ₁	A ₀	RE	WE																				
0	0	Status Register	Command Register																				
0	1	Track Register	Track Register																				
1	0	Sector Register	Sector Register																				
1	1	Data Register	Data Register																				
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit inverted bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by WE or a transmitter enabled by RE.																				
24	CLOCK	CLK	This input requires a free-running 2 MHz ± 1% square wave clock for internal timing reference.																				
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.																				
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.																				
Floppy Disk Interface:																							
15	Phase 1/Step	PH1/STEP	If the 3PM input is a logic low the three-phase motor control is selected and PH1, PH2, and PH3 outputs form a one active low signal out of three. PH1 is active low after MR. If the 3PM input is a logic high the step and direction motor control is selected. The step output contains a 4 usec high signal for each step and the direction output is active high when stepping in; active low when stepping out.																				
16	Phase 2/Direction	PH2/DIRC																					
17	Phase 3	PH3																					
18	3-Phase Motor Select	3PM																					

Pin No.	Pin Name	Symbol	Function
22	TEST	TEST	This input is used for testing purposes only and should be tied to +5V or left open by the user.
23	HEAD LOAD TIMING	HLT	The HLT input is sampled after 10 ms. When a logic high is sampled on the HLT input the head is assumed to be engaged.
25	EXTERNAL DATA SEPARATION	XTDS	A logic low on this input selects external data separation. A logic high or open selects the internal data separator.
26	FLOPPY DISK CLOCK (External Separation)	FDCLOCK	This input receives the externally separated clock when XTDS = 0. If XTDS = 1, this input should be tied to a logic high.
27	FLOPPY DISK DATA	FDDATA	This input receives the raw read disk data if XTDS=1, or the externally separated data if XTDS=0.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	Track Greater than 43	TG43	This output informs the drive that the Read-Write head is positioned between tracks 44-76. This output is valid only during Read and Write commands.
30	WRITE GATE	WG	This output is made valid when writing is to be performed on the diskette.
31	WRITE DATA	WD	This output contains both clock and data bits of 500 ns duration.
32	Ready	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low, the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE FAULT	WF	This input detects wiring faults indications from the drive. When WG=1 and WF goes low, the current Write command is terminated and the Write Fault status bit is set. The WF input should be made inactive (high) when WG becomes inactive.
34	TRACK 00	TR00	This input informs the FD1771 that the Read-Write head is positioned over Track 00 when a logic low.
35	INDEX PULSE	IP	Input, when low for a minimum of 10 usec, informs the FD1771 when an index mark is encountered on the diskette.
36	WRITE PROTECT	WPRT	This input is sampled whenever a Write command is received. A logic low terminates the command and sets the Write Protect status bit.
37	DISK INITIALIZATION	DINT	The input is sampled whenever a Write Track command is received. If DINT=0, the operation is terminated and the Write Protect status bit is set.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 4. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register: This 8-bit register assembles serial data from the Read Data input (FDDATA) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register: This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register: This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be

loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR): This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR): This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR): This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic: This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU): The ALU is a serial comparator, incrementer, and decremter and is used for register modification and comparisons with the disk recorded ID field.

AM Detector: The Address Mark detector is used to detect ID, Data, and Index address marks during Read and Write operations.

Timing and Control: All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from a 2.0 MHz external crystal clock.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1771. The DAL are three-state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The least-significant address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1-A0	READ (RE)	WRITE (WE)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1771 and the Processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded

at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. A 2.0 MHz $\pm 1\%$ square wave clock is required at the CLK input for internal control timing (may be 1.0 MHz for mini floppy).

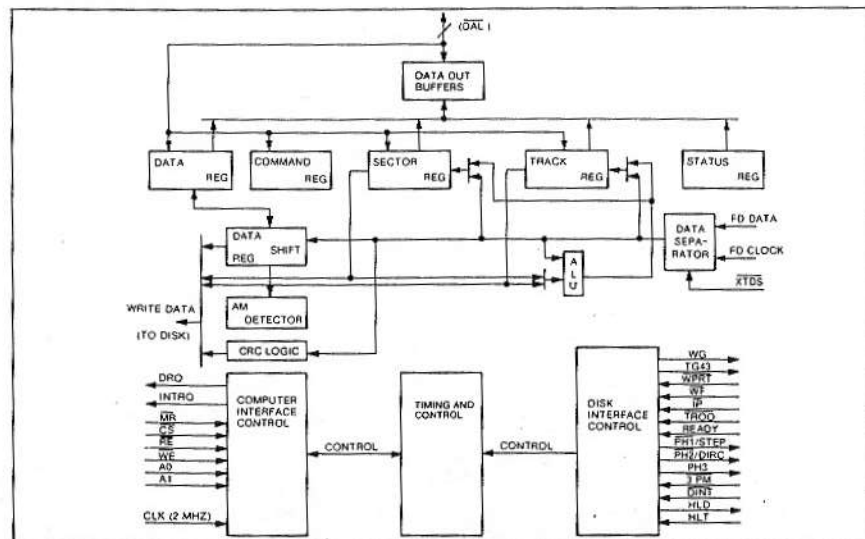
HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step, an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Three-Phase Motor or a Step-Direction Motor through the device interface. When the 3PM input is connected to ground, the device operates with a three-phase motor control interface, with one active low signal per phase on the three output signals PH1, PH2, and PH3. The stepping sequence, when stepping in, is Phases 1-2-3-1, and when stepping out, Phases 1-3-2-1. Phase 1 is active low after Master Reset. Note: PH3 needs an inverter if used.

The Step-Direction Motor Control interface is activated by leaving input 3PM open or connecting it to +5V. The Phase 1 pin PH1 becomes a Step pulse of 4 microseconds width. The Phase 2 pin PH2 becomes a direction control with a high voltage on this pin indicating a Step In, and a low voltage indicating a Step Out. The Direction output is valid a minimum of 24 μ s prior to the activation of the Step pulse.

When a Seek, Step or Restore command is executed, an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not



FD1771 BLOCK DIAGRAM

made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is reset.

Table 1. STEPPING RATES

r ₁	r ₀	1771-X1 CLK = 2 MHz TEST = 1	1771-X1 CLK = 1 MHz TEST = 1	1771 or -X1 CLK = 2 MHz TEST = 0	1771 or -X1 CLK = 1 MHz TEST = 0
0	0	6ms	12ms	Approx. 400µs*	Approx. 800µs*
0	1	6ms	12ms		
1	0	10ms	20ms		
1	1	20ms	40ms		

*For exact times consult WDC.

The Head Load (HLD) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify operation, or a Seek or Step operation with the head load bit, h, a logic one remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HLD signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input after 10 msec. A high state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded after stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The 2.0 MHz external clock provided to the device is internally divided by 4 to form the 500 kHz clock rate for data transfer. When reading data from a diskette this divider is synchronized to transitions of the Read Data (FDDATA) input. When a transition does not occur on the 500 kHz clock active state, the clock divider circuit injects a clock to maintain a continuous 500 kHz data clock. The 500 kHz data clock is further divided by 2 internally to separate the clock and information bits. The divider is phased to the information by the detection of the address mark.

In the internal data read and separation mode the Read Data input toggles from one state to the opposite state for each logic one bit of clock or information. This signal can be derived from the amplified, differentiated, and sliced Read Head signal, or by the output of a flip-flop toggling on the Read Data pulses. This input is sampled by the 2 MHz clock to detect transitions.

The chip can also operate on externally separated

data, as supplied by methods such as Phase Lock loop, One Shots, or variable frequency oscillators. This is accomplished by grounding the External Data Separator (XTDS) INPUT. When the Read Data input makes a high-to-low transition, the information input to the FDDATA line is clocked into the Data Shift Register. The assembled 8-bit data from the Data Shift Register are then transferred to the Data Register.

The normal sector length for read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read and Write commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands, respectively, by setting a logic 0 in Bit 3 of the command word. The sector length indicator specifies the number of 16 byte groups or 16 x N, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 µsec duration. This signal may be used to externally toggle a flip-flop to control the direction of Write Current flow.

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request from the FD1771 before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1771 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

Whenever a Read or Write command is received the FD1771 samples the READY input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the READY input.

COMMAND DESCRIPTION

The FD1771 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault-free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

TYPE 1 COMMANDS

The Type 1 Commands include the RESTORE, SEEK, STEP, STEP-IN, and STEP-OUT commands. Each of the Type 1 Commands contain a rate field (r₀r₁), which determines the stepping motor rate as defined in Table 1, page 4.

The Type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output is made active). If h=0, HLD is deactivated.

Table 2. COMMAND SUMMARY

TYPE	COMMAND	BITS							
		7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	v	r ₁	r ₀
I	Seek	0	0	0	1	h	v	r ₁	r ₀
I	Step	0	0	1	u	h	v	r ₁	r ₀
I	Step In	0	1	0	u	h	v	r ₁	r ₀
I	Step Out	0	1	1	u	h	v	r ₁	r ₀
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a ₁ a ₀	
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	1	0	0
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	t ₃	t ₂	t ₁	t ₀

Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I
<u>h</u> = Head Load flag (Bit 3)
h = 1, Load head at beginning
h = 0, Do not load head at beginning
<u>V</u> = Verify flag (Bit 2)
V = 1, Verify on last track
V = 0, No verify
<u>r₁r₀</u> = Stepping motor rate (Bits 1-0)
Refer to Table 1 for rate summary
<u>u</u> = Update flag (Bit 4)
u = 1, Update Track register
u = 0, No update

Table 4. FLAG SUMMARY

TYPE II
<u>m</u> = Multiple Record flag (Bit 4)
m = 0, Single Record
m = 1, Multiple Records
<u>b</u> = Block length flag (Bit 3)
b = 1, IBM format (128 to 1024 bytes)
b = 0, Non-IBM format (16 to 4096 bytes)
<u>a₁a₀</u> = Data Address Mark (Bits 1-0)
a ₁ a ₀ = 00, FB (Data Mark)
a ₁ a ₀ = 01, FA (User defined)
a ₁ a ₀ = 10, F9 (User defined)
a ₁ a ₀ = 11, F8 (Deleted Data Mark)

Table 5. FLAG SUMMARY

TYPE III
<u>s</u> = Synchronize flag (Bit 0)
s = 0, Synchronize to AM
s = 1, Do Not Synchronize to AM
TYPE IV
<u>li</u> = Interrupt Condition flags (Bits 3-0)
li = 1, Not Ready to Ready Transition
li = 1, Ready to Not Ready Transition
li = 1, Index Pulse
li = 1, Immediate interrupt
E = Enable HLD and 10 msec Delay
E = 1, Enable HLD, HLT and 10 msec Delay
E = 0, Head is assumed Engaged and there is no 10 msec Delay

Once the head is loaded, the head will remain engaged until the FD1771 receives a command that specifically disengages the head. If the FD1771 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type 1 Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed; if V=0, no verification is performed.

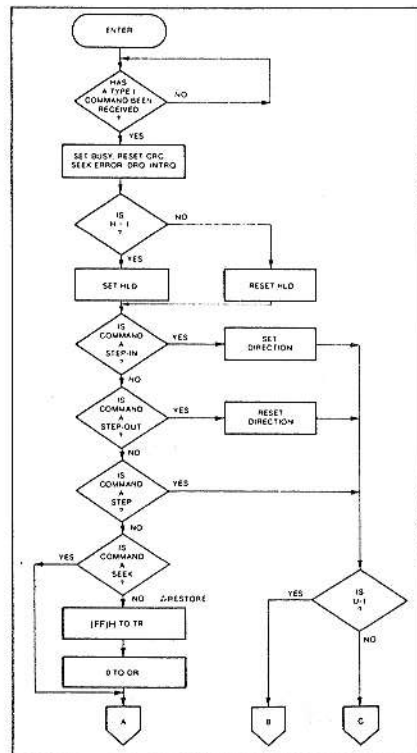
During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID Field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the BUSY status bit is reset. If there is not a match but there is

valid ID CRC, an interrupt is generated, the Seek Error status bit (Status Bit 4) is set and the BUSY status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status Bit 3), and the next encountered ID Field is read from the disk for the verification operation. If an ID Field with a valid CRC cannot be found after two revolutions of the disk, the FD1771 terminates the operation and sends an interrupt (INTRQ).

The STEP, STEP-IN, and STEP-OUT commands contain an UPDATE flag (U). When U=1, the track register is updated by one for each step. When U=0, the track register is not updated.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track

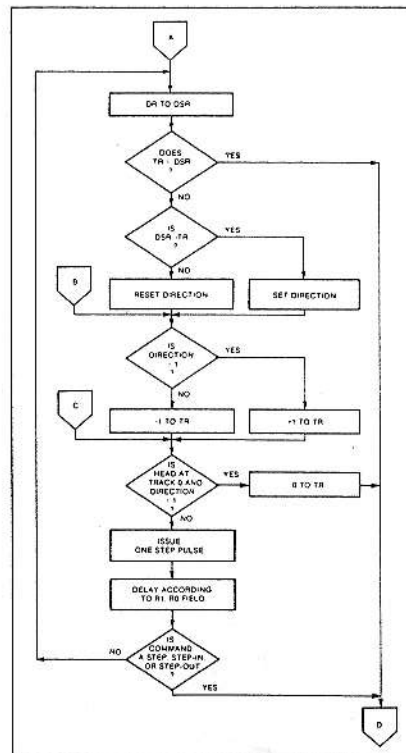


TYPE I COMMAND FLOW

Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r_{1r0} field are issued until the $\overline{TR00}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD1771 terminates operation, interrupts, and sets the Seek error status bit. Note that the RESTORE command is executed when MR goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1771 will update the



TYPE I COMMAND FLOW

Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1771 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_{1r0} field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An

interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_{1r0} field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r_{1r0} field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

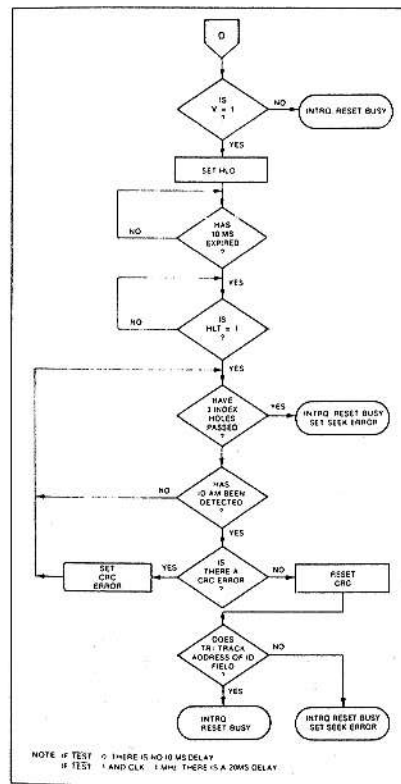
TYPE II COMMANDS

The Type II Commands include the Read Sector(s) and Write Sector(s) commands. Prior to loading the Type II command into the COMMAND REGISTER, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy status bit is set. If the E flag=1 (this is the normal case), HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and the Data Field format are shown below.

When an ID field is located on the disk, the FD1771 compares the track number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending on the command. The FD1771 must find an ID field with a track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record Not Found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where $n = 0, 1, 2, 3$.



NOTE: IF TEST 0, THERE IS NO 10 MSEC DELAY
IF TEST 1 AND CLK. 1 MHz, THERE IS A 20MS DELAY

TYPE II COMMAND FLOW

GAP	ID AM	TRACK NUMBER	ZERO	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD								DATA FIELD				

IDAM = ID Address Mark — DATA = (FE)₁₆ CLK = (C7)₁₆
 Data AM = Data Address Mark — DATA = (F8, F9, FA, or FB), CLK = (C7)₁₆

For b = 1

Sector Length Field (Hex)	Number of Bytes in Sector (Decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below.

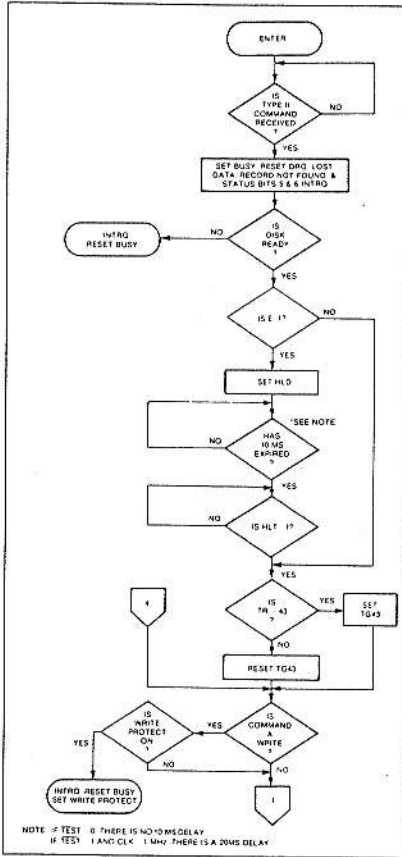
For b = 0

Sector Length Field (Hex)	Number of Bytes in Sector (Decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
•	•
FF	4080
00	4096

Each of the Type II commands also contain a (m) flag which determines if the multiple records (sectors) are to be read or written, depending upon the command. If m=0 a single sector is read or written and an interrupt is generated at the completion of the command. If m=1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1771 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the command register, which terminated the command and generates an interrupt.

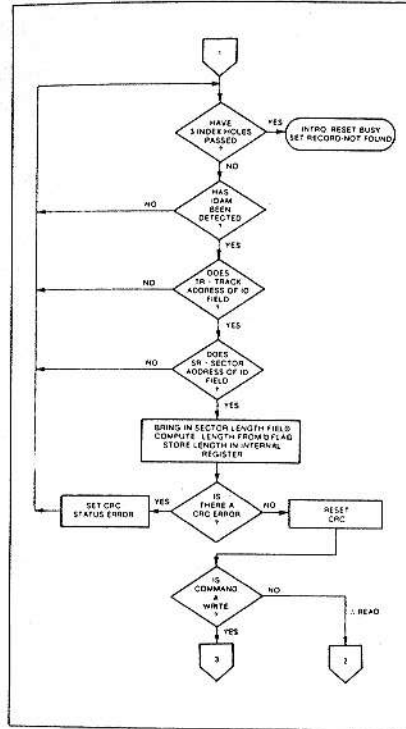
READ COMMAND

Upon receipt of the Read command, the head is loaded, the BUSY status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct field; if not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been



TYPE II COMMAND FLOW

shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the

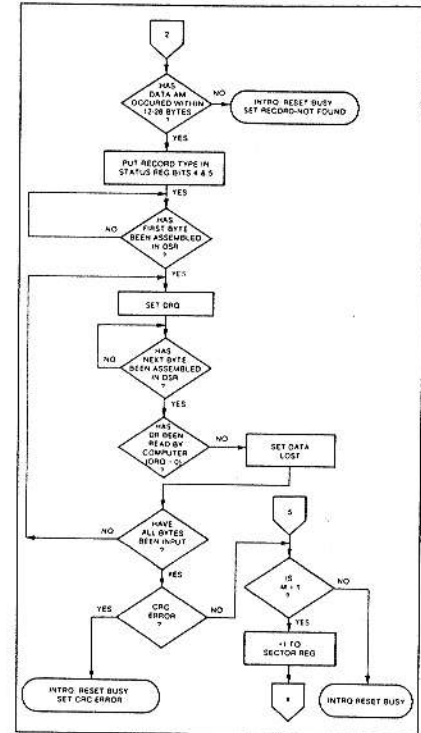


TYPE II COMMAND FLOW

Lost Data status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below.

Status Bit 6	Status Bit 5	Data AM (Hex)
0	0	FB
0	1	FA
1	0	F9
1	1	F8



TYPE II COMMAND FLOW

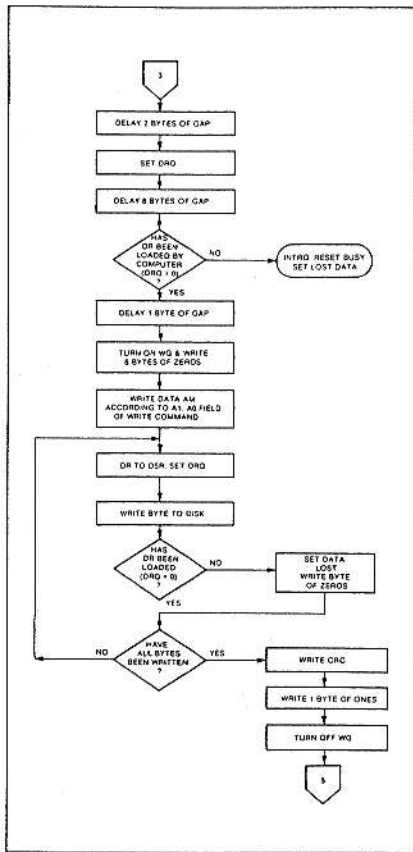
WRITE COMMAND

Upon receipt of the Write command, the head is loaded (HLD active) and the BUSY status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1771 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a₁a₀ field of the command as shown on next page.

The FD1771 then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in

a ₁	a ₀	Data Mark (Hex)	Clock Mark (Hex)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

time for continuous writing the Lost Data status bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.



TYPE II COMMAND FLOW

TYPE III COMMANDS

READ Address

Upon receipt of the Read Address command, the head is loaded and the BUSY Status bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below.

TRACK ADDRESS	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

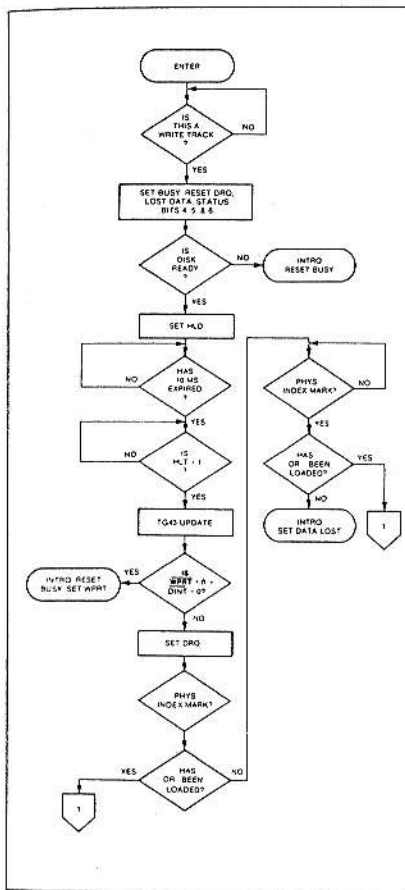
Although the CRC characters are transferred to the computer, the FD1771 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the Sector Register. At the end of the operation an interrupt is generated and the BUSY Status is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the BUSY status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit 0(S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

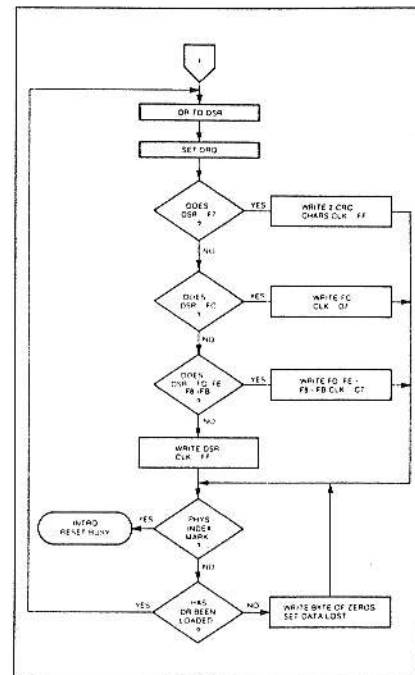
Upon receipt of the Write Track command, the head is loaded and the BUSY status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data status bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.



TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Character	C7
F8	Data Address Mark	C7
F9	Data Address Mark	C7
FA	Data Address Mark	C7
FB	Data Address Mark	C7
FC	Index Address Mark	D7
FD	Spare	
FE	ID Address Mark	C7



TYPE III COMMAND WRITE TRACK

The Write Track Command will not execute if the DINT input is grounded; instead, the Write Protect status bit is set and the interrupt is activated. Note that one F7 pattern generates two CRC characters.

TYPE IV COMMAND

Force Interrupt

This command can be loaded into the command register at any time. If there is a current command under execution (BUSY status bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I₀ through I₃ field is detected. The interrupt conditions are shown below:

- I₀ = Not-Ready-To-Ready Transition
- I₁ = Ready-To-Not-Ready Transition
- I₂ = Every Index Pulse
- I₃ = Immediate Interrupt (Requires reset, see Note)

NOTE: If I₀ - I₃ = 0, there is no interrupt generated but the current command is terminated and busy is reset. This is the only command that will clear the immediate interrupt.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is

reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below.

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

Table 6. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	0
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE PROTECT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	WRITE FAULT
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the READY input and logically "ored" with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2	TRACK 00	When set, indicates Read-Write head is positioned to Track 0. This bit is an inverted copy of the TR00 input.
S1	INDEX	When set, indicates Index mark detected from drive. This bit is an inverted copy of the IP input.
S0	BUSY	When set, command is in progress. When reset, no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the READY input and "ored" with MR. The TYPE II and III Commands will not execute unless the drive is ready.
S6	RECORD TYPE/ WRITE PROTECT	On Read Record: It indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Protect. This bit is reset when updated.
S5	RECORD TYPE/WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Ready operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0	BUSY	When set, command is under execution. When reset, no command is under execution.

FORMATTING THE DISK (Refer to section on Type III Commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD1771 raises the Data Request signal. At this point in time, the user loads the Data Register with desired data to be written on the disk. For every byte of information to be written on the disk, a Data Request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the Data Register is written on the disk with a clock mark of (FF)₁₆. However, if the FD1771 detects a data pattern on F7 through FE in the Data Register, this is interpreted as data address marks with missing clocks or CRC generation. For

instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 through FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128, 256, 512, or 1024 bytes, or may be formatted in non-IBM format with sector lengths of 16 to 4096 bytes in 16-byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes/sector. The next section deals with the IBM 3740 format with 128 bytes/sector followed by a section of non-IBM formats.

IBM 3740 Formats — 128 Bytes/Sector

The IBM format with 128 bytes/sector is depicted in the Track Format figure on the following page. In order to create this format, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

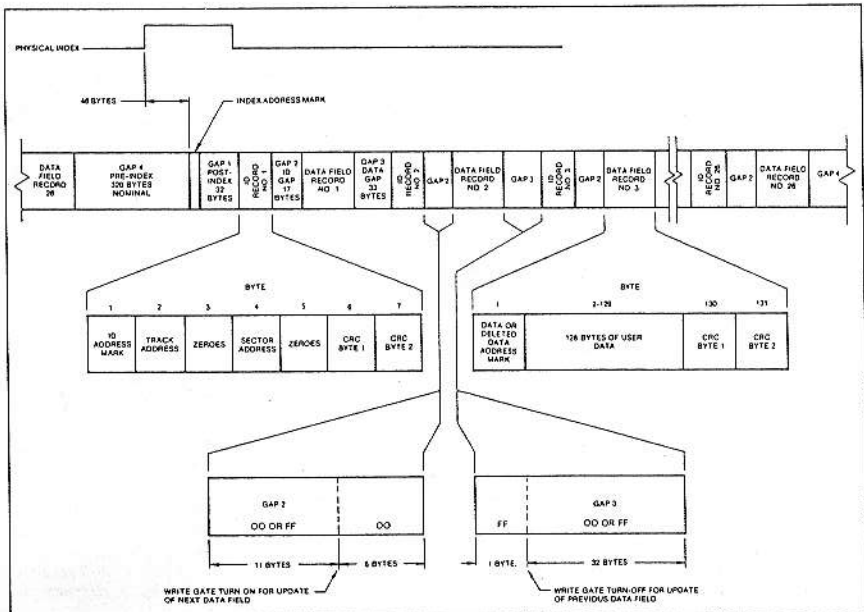
Number of Bytes	Hex Value of Byte Written
40	00 or FF
6	00
1	FC (Index Mark)
26	00 or FF
6	00
1	FE (ID Address Mark)
1	Track Number (0 through 4C)
1	00
1	Sector Number (1 through 1A)
1	00
1	F7 (two CRCs written)
11	00 or FF
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (two CRCs written)
27	00 or FF
247**	00 or FF

*Write bracketed field 26 times.
 **Continue writing until FD1771 interrupts out.
 Approximately 247 bytes.

Non-IBM Formats
 Non-IBM formats are very similar to the IBM formats except a different algorithm is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to Section V, Type II commands with b flag equal to zero. Note that F7 through FE must not appear in the sector length byte of the ID field.

In formatting the FD1771, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field) must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The FD1771 does not require the index address mark (i.e., DATA = FC, CLK = D7) and need not be present.

- References:**
- 1) IBM Diskette OEM Information GA21-9190-1.
 - 2) SA900 IBM Compatibility Reference Manual — Shugart Associates.



TRACK FORMAT

ELECTRICAL CHARACTERISTICS

Maximum Ratings
 V_{DD} with respect to V_{BB} (Ground) -20 to -0.3V
 Max Voltage to any input with respect to V_{BB} -20 to -0.3V
 Operating Temperature 0°C to 70°C
 Storage Temperature -55°C to +125°C

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C. V_{DD} = +12.0V ± 6V.
 V_{BB} = -5.0 ± 5V. V_{SS} = 0V. V_{CC} = -5V ± 25V
 I_{DD} = 10 ma Nominal, I_{CC} = 30 ma Nominal,
 I_{BB} = 0.4 μa Nominal

Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
I _{LI}	Input Leakage			10	μA	V _{IN} = V _{DD}
I _{LO}	Output Leakage			10	μA	V _{OUT} = V _{DD}
V _{IH}	Input High Voltage	2.6			V	
V _{IL}	Input Low Voltage (All Inputs)			0.8	V	
V _{OH}	Output High Voltage	2.8			V	I _O = -100 μA
V _{OL}	Output Low Voltage			0.45	V	I _O = 1.0 mA

TIMING CHARACTERISTICS

T_A = 0°C to 70°C. V_{DD} = +12V ± 6V.
 V_{BB} = -5V ± 25V. V_{SS} = 0V. V_{CC} = -5V ± 25V

NOTE: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz. Use 1 MHz when using mini-floppy.

Read Operations

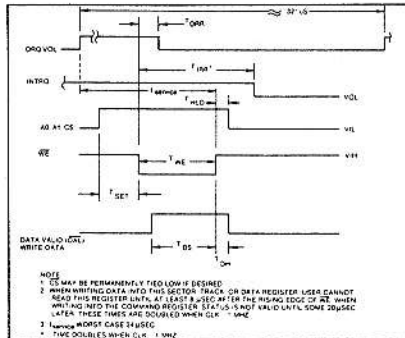
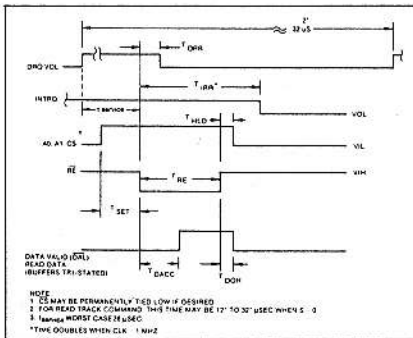
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TSET	Setup ADDR and CS to \overline{RE}	100			nsec	
THLD	Hold ADDR and CS from \overline{RE}	10			nsec	
TRE	\overline{RE} Pulse Width	450			nsec	C _L = 25 pf
TDRR	DRQ Reset from \overline{RE}			750	nsec	
TIRR	INTRO Reset from \overline{RE}			3000	nsec	
TDACC	Data Access from \overline{RE}			450	nsec	C _L = 25 pf
TDOH	Data Hold from \overline{RE}	50		150	nsec	C _L = 25 pf

Write Operations

Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TSET	Setup ADDR and CS to \overline{WE}	100			nsec	
THLD	Hold ADDR and CS from \overline{WE}	10			nsec	
TWE	\overline{WE} Pulse Width	450	300		nsec	
TDRR	DRQ Reset from \overline{WE}			750	nsec	
TIRR	INTRO Reset from \overline{WE}			3000	nsec	See Note
TDS	Data Setup to \overline{WE}	350			nsec	
TDH	Data Hold from \overline{WE}	150			nsec	

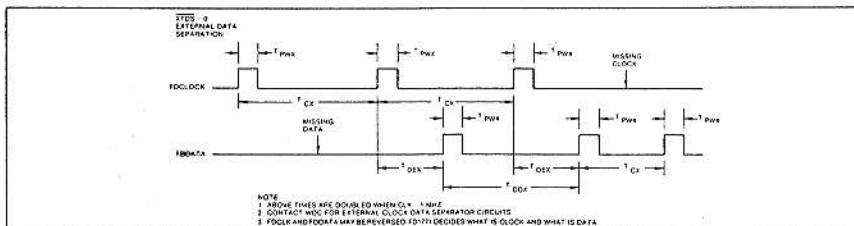
External Data Separation (XTDS = 0)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TPWX	Pulse Width Read Data & Read Clock	150		350	nsec	
TCX	Clock Cycle External	2500			nsec	
TDEX	Data to Clock	500			nsec	
TDDX	Data to Data Cycle	2500			nsec	



READ ENABLE TIMING

WRITE ENABLE TIMING



READ TIMING (XTDS = 0)

Internal Data Separation (XTDS = 1)

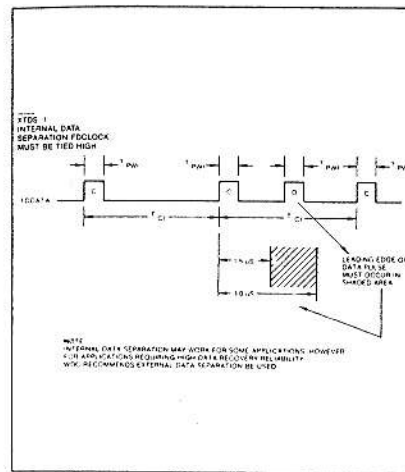
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TPWI	Pulse Width Data and Clock	150		1000	nsec	
TCI	Clock Cycle Internal	3500		5000	nsec	

Write Data Timing

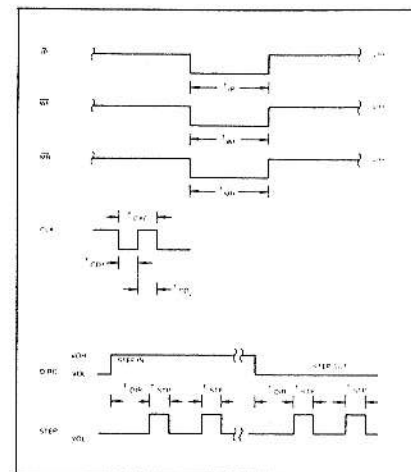
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TWGD	Write Gate to Data		1200		nsec	300 nsec \pm CLK tolerance
TPWW	Pulse Width Write Data	500		600	nsec	
TCDW	Clock to Data		2000		nsec	\pm CLK tolerance
TCW	Clock Cycle Write		4000		nsec	\pm CLK tolerance
TWGH	Write Gate Hold to Data	0		100	nsec	

Miscellaneous Timing

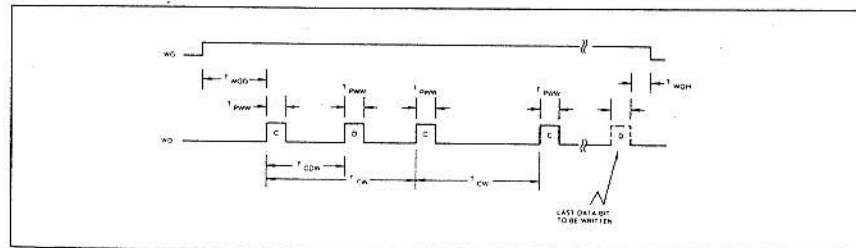
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TCD ₁	Clock Duty	175			nsec	2 MHz \pm 1% See Note
TCD ₂	Clock Duty	210			nsec	
TSTP	Step Pulse Output	3800		4200	nsec	These times doubled when CLK = 1 MHz
TDIR	Direct Setup to Step	24			nsec	
TMR	Master Reset Pulse Width	10			nsec	
TIP	Index Pulse Width	10			nsec	
TWF	Write Fault Pulse Width	10			nsec	



READ TIMING (XTDS = 1)



MISCELLANEOUS TIMING



WRITE DATA TIMING

1771-01 Application Notes

INTRODUCTION

The FD1771-01 Floppy Disk Formatter/Controller is a MOS/LSI device designed to ease the task of interfacing the 8" or 5¼" (mini-floppy) disk drive to a host processor. It is ideally suited for a wide range of microprocessors, providing an 8-bit bi-directional interface to the CPU for all control and data transfers. Requiring standard +12, ±5V power supplies, the 1771 is available in ceramic or plastic 40 pin dual-in-line packages.

The 1771 has been designed to be compatible with the IBM 3740 standard. This single-density Frequency Modulated (FM) recording technique, records a clock bit between a data bit serially on each track. Figure 1 illustrates how a HEX "D2" is recorded. Note that when the data bit to be written is zero, no pulse or flux transition is recorded. For the 8" drive, there are 77 tracks, with 26 sectors on each track. Each sector contains 128 bytes of data. Although there is no "standard" format for the mini-floppy, most manufacturers utilize either 35 or 40 tracks per side, with 16 sectors of 128 bytes each per track. Both the 8" and 5¼" formats must be soft-sectored, i.e., there are no physical holes to denote sector locations. The hard-sectored disk has been losing popularity, mainly due to the fact that the sector lengths cannot be increased.

Being soft-sector compatible, the 1771 must know where each sector begins on the track. This is performed by using Address Marks. These bytes are recorded on the disk with certain clock pulses missing, and are unique from all other data and gap bytes recorded on the track. Six distinct Address Marks can be used:

Description	Data	Clock Pattern
Index Address Mark	FC	D7
ID Address Mark	FE	C7
Data Address Mark	FB	C7
User defined	FA	C7
User Defined	F9	C7
Deleted Address Mark	F8	C7

The two "User Defined" Address Marks are unique to the 1771, and do not appear in the IBM 3740 standard. These Address Marks can be used to

define the type of data i.e., "object" or "text" data, alternate sector data, or any other purpose the user chooses.

PROCESSOR INTERFACE

The 1771 contains five internal registers that can be accessed via the 8-bit DAL lines by the CPU. These registers are used to control the movement of the head, read and write sectors, and perform all other functions at the drive. Regardless of the operation performed, it must be initiated through one or more of these registers. They are selected by a proper binary code on the A0, A1 lines in conjunction with the \overline{RE} and \overline{WE} lines when the device is selected. The registers and their addresses are:

\overline{CS}	A ₁	A ₀	$\overline{RE} = 0$	$\overline{WE} = 0$
0	0	0	STATUS REG	COMMAND REG
0	0	1	TRACK REG	TRACK REG
0	1	0	SECTOR REG	SECTOR REG
0	1	1	DATA REG	DATA REG
1	X	X	Deselected	Deselected

Command Register: This is a write-only register used to send all commands to the 1771.

Status Register: This is a read-only register that must be read at the completion of every command to determine whether execution was successful. It may also be used to monitor command execution, and to sense when data is required by the drive for read or write operations.

Track Register: This R/W register holds the current position of the R/W head.

Sector Register: This R/W register holds the desired sector number for read and write commands.

Data Register: This R/W register contains the data to be read or written to a particular sector.

INTERRUPTS

There are two INTERRUPT lines for CPU use. These are the DRQ (Data Request) and INTRQ (Interrupt Request). These are active high, open drain outputs and require a pull-up resistor of 10K or greater to +5V. Both of these signals also appear in the status register as the Busy (INTRQ) and the data request (DRQ) bits. The user has the option of utilizing these hardware lines for system interrupts, or through

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software by polling the status register. The choice is dependent upon the particular microprocessor and support hardware of the system.

INTRQ: This line is used to signify the completion of any command. It is reset low when a new command is loaded into the command register, or when the status register is read.

DRQ: This line is active high whenever the data register requires servicing. During a read command, it signifies that the data register contains a byte of data from the disk and may be read by the CPU. During a write command, it signifies that the data register is empty and may be loaded with the next byte to be written on the disk. The DRQ line is reset whenever the data register is read or written to. It is also reset when a new command is loaded into the command register, providing the new command is not a Forced Interrupt, and the 1771 is not busy (Busy Bit = 0).

WRITE SECTOR

With the use of the WRITE SECTOR command, the CPU can access any desired sector(s) in a track. Prior to loading this command, the R/W head of the drive must be positioned over the specific track. This can be first accomplished with the use of any of the Type I commands. Once positioned, the CPU must load the desired sector number into the sector register, then issue the command. The head will load, and the 1771 will begin searching for the correct ID field. If the correct sector and track is not found within 2 revolutions of the disk, the RECORD-NOT-FOUND bit will be set in the status register, and the command will be terminated. Once found, the 1771 will issue a DRQ in request of the first data byte to be written. Once the data register is loaded, the 1771 will issue a DRQ for each byte to be recorded, until the entire sector is written. For the 8" drive, the user must load the data register 24 microseconds after a DRQ is generated. Failure to meet this time will cause the lost data bit to be set, and a byte of zeros substituted and written on the disk.

READ SECTOR

The READ SECTOR command functions in much the same way as the WRITE SECTOR command. The sector register must again be loaded with the desired sector number, before the read command can be loaded. After the ID field has been found, the 1771 will begin generating DRQ's, with the data register being loaded with each byte of the sector field. For the 8" drive, the user must read the data register at least 26 microseconds after the DRQ is generated. Failure to meet this time will cause the lost data bit to be set in the status register, while the next assembled byte will overwrite the contents of the data register.

Both the Read and Write sector commands also

contain an "m" flag for accessing multiple sectors. The sector register is incremented internally after each sector is read or written to. Eventually the sector register will exceed the physical number of sectors on the track. The user can either issue the Forced Interrupt command after the last sector, or wait for the 1771 to interrupt out. In the latter case, the RECORD-NOT-FOUND status bit will be set.

FLOPPY DISK INTERFACE

For the most part, the actual Floppy Disk Interface will consist mainly of Buffer/Drivers. Most drives manufactured today require an open collector TTL interface, with appropriate resistor terminal networks. Figure 2 shows the interface of the 1771 to a Shugart SA400 Drive. Aside from the data separator, the interface consists mainly of 7438's and 7414 TTL gates. A 9602 one-shot is used for the desired head load delay. In this illustration, the 6800 microprocessor is used via a 6820 Peripheral Interface Adapter to control all functions of the 1771. Similarly, other parallel port devices (such as the 8255 for 8080 systems) can be used for the interface, or the 1771 may simply be tied directly to the systems data bus and control lines, providing TTL loading factors are observed.

DATA SEPERATION

The internal DATA SEPERATOR of the 1771 can be used by tying the XTDS line high, and supplying the combined clock and data pulses on the FD data line. In order to maintain an error rate better than 1×10^9 , and external data separator is recommended.

Since the 1771 system clock is at 2 MHz, this allows for a 500 ns resolution. The internal data window will move 500 ns with respect to the incoming data bit. On the inner tracks of the drive, the bit shift is more severe and may occasionally cause a data or clock bit to fall outside of this data window. Since the 1771 will perform up to 5 retries, this error rate may be acceptable for some applications.

When the XTDS line is forced low, the 1771 will accept separated clock and data on the FDCLOCK and FDDATA lines. Figure 3 illustrates the timing of these signals. The actual FDCLOCK and FDDATA lines may be reversed; the 1771 will determine which line is clock and which is data when an Address Mark is detected. This feature greatly simplifies the design of the data separator.

Figure 4 illustrates the Phase-Lock Loop method for data separation. The circuit operates at 8 MHz, or 32 times the frequency of a received bit cell. The MC4024 VCO is used to supply the nominal clock frequency. The first 74LS161 counter provides a divide by 16 frequency and a carry to one side of the MC4044 phase detector. The other input of the MC4044 is tied to another 74LS161 counter which is affected by the incoming data stream. The output of

the phase detector is a signal proportional to the differences of the incoming pulses. This is then fed through a low pass filter, and to the input of the MC4024 to adjust the output frequency. Figures 5 thru 8 illustrate other types of data separators.

These employ the "Counter Separator" techniques and are quite different from the Phase-Lock-Loop method. With the addition of "One-Shot" delay element or an input clock, most of the complexity of the PPL circuit can be eliminated.

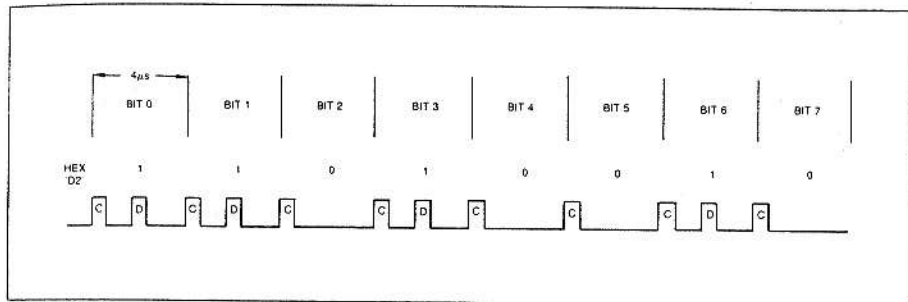


FIGURE 1. FM RECORDING.

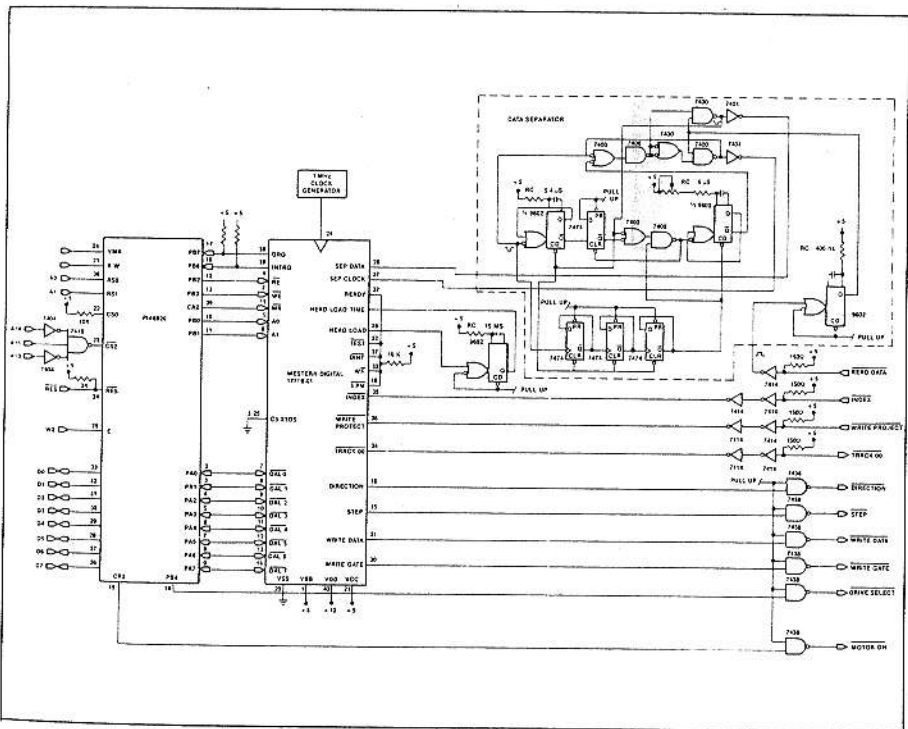


FIGURE 2. 1771 TO SHUGART SA400 DRIVE

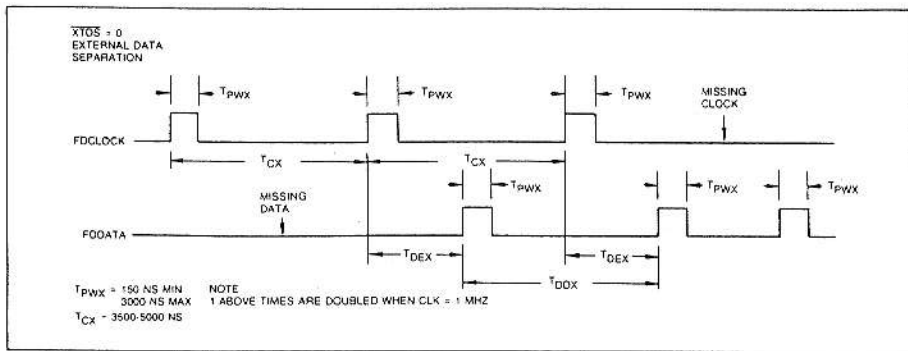


FIGURE 3. EXTERNAL DATA SEPARATOR TIMING.

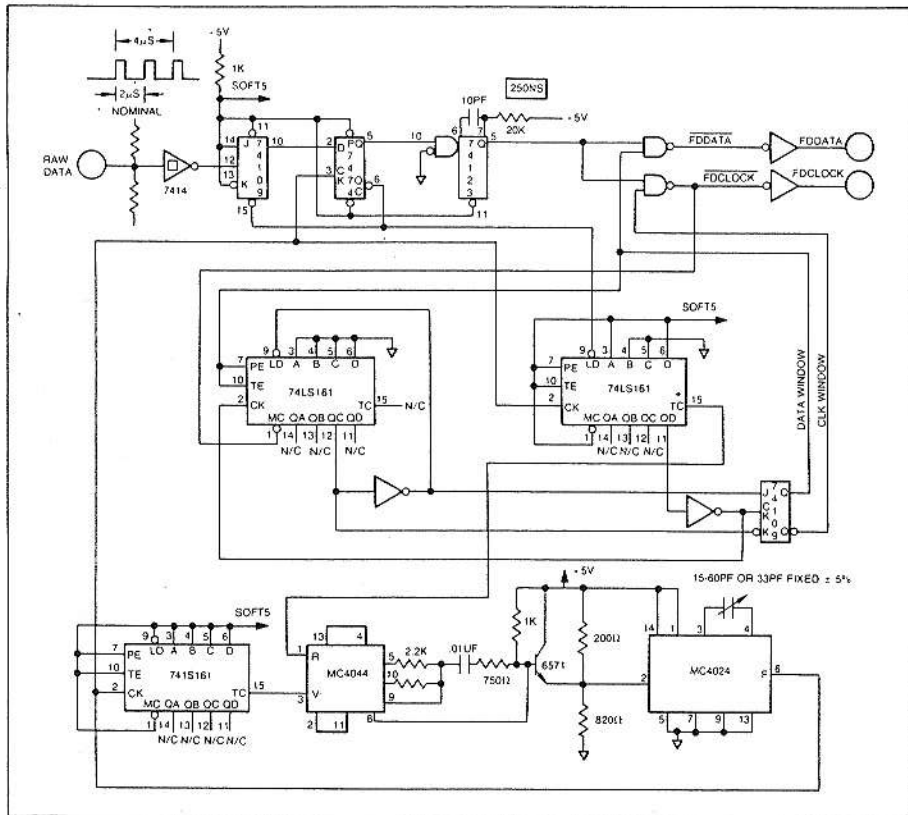


FIGURE 4. CIRCUIT PROVIDED COURTESY OF MOTOROLA AND ICOM CORPS.

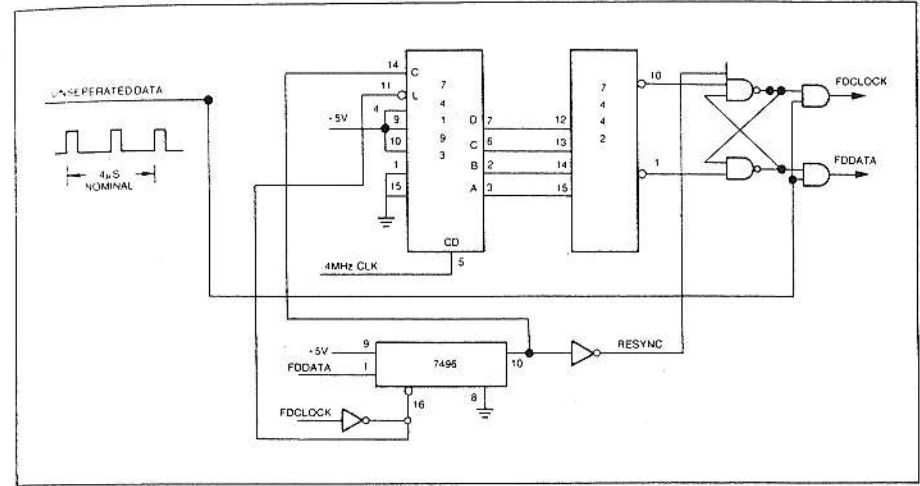


FIGURE 5. CIRCUIT PROVIDED COURTESY OF PROCESSOR APPLICATIONS LTD.

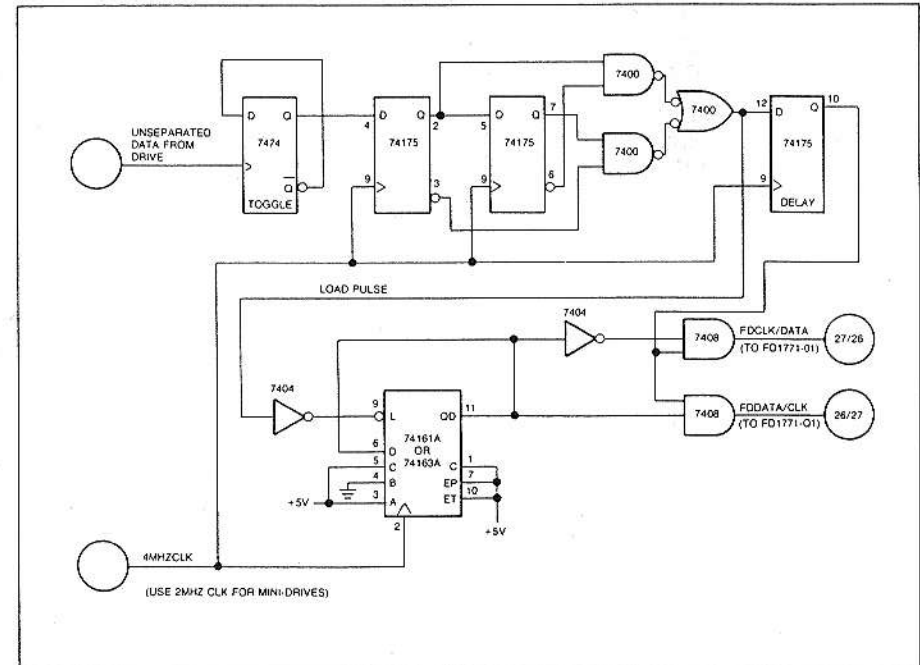


FIGURE 6.

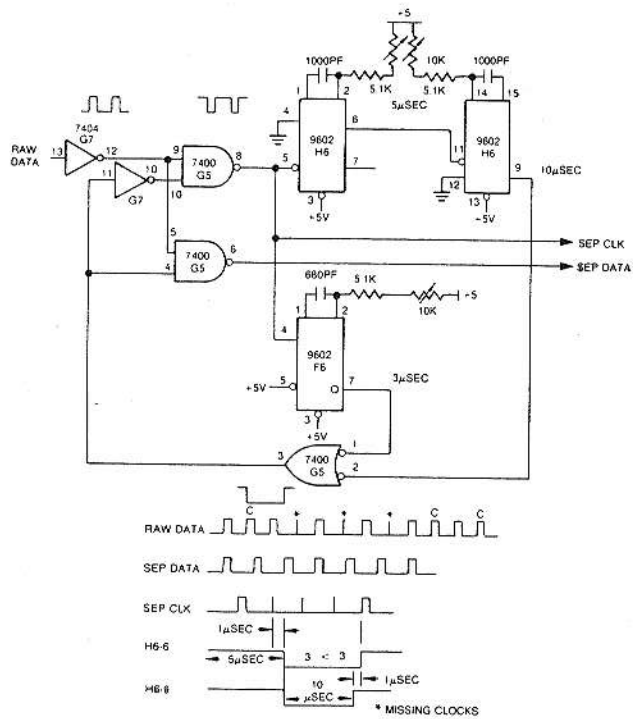


FIGURE 7. CIRCUIT PROVIDED COURTESY OF ACUTEST CORP.

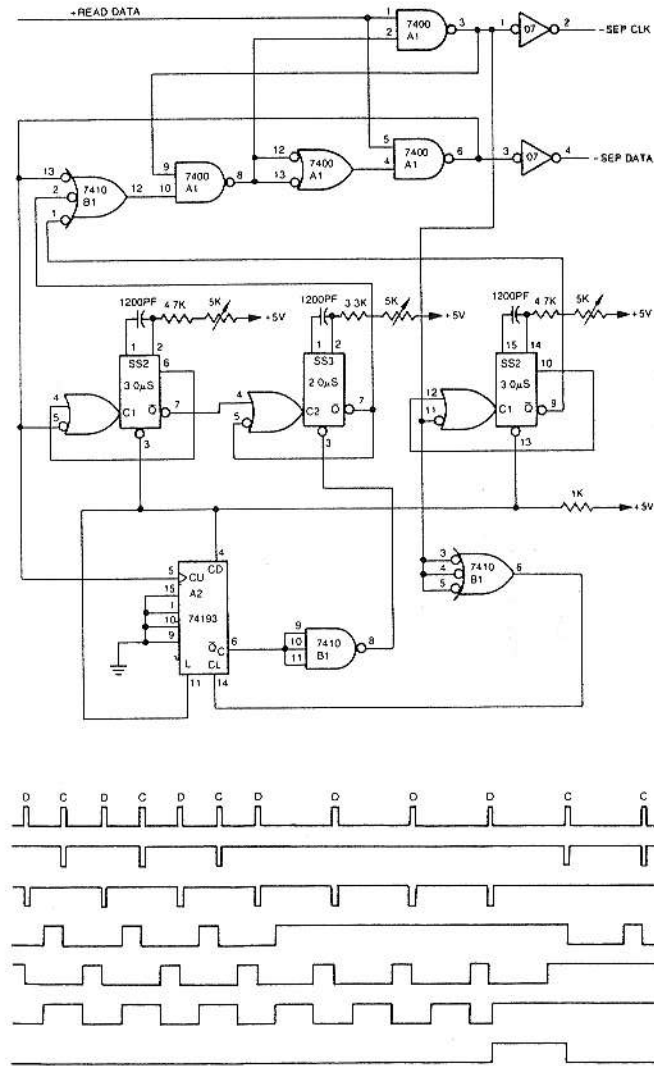


FIGURE 8. CIRCUIT PROVIDED COURTESY OF SHUGART ASSOCIATES.