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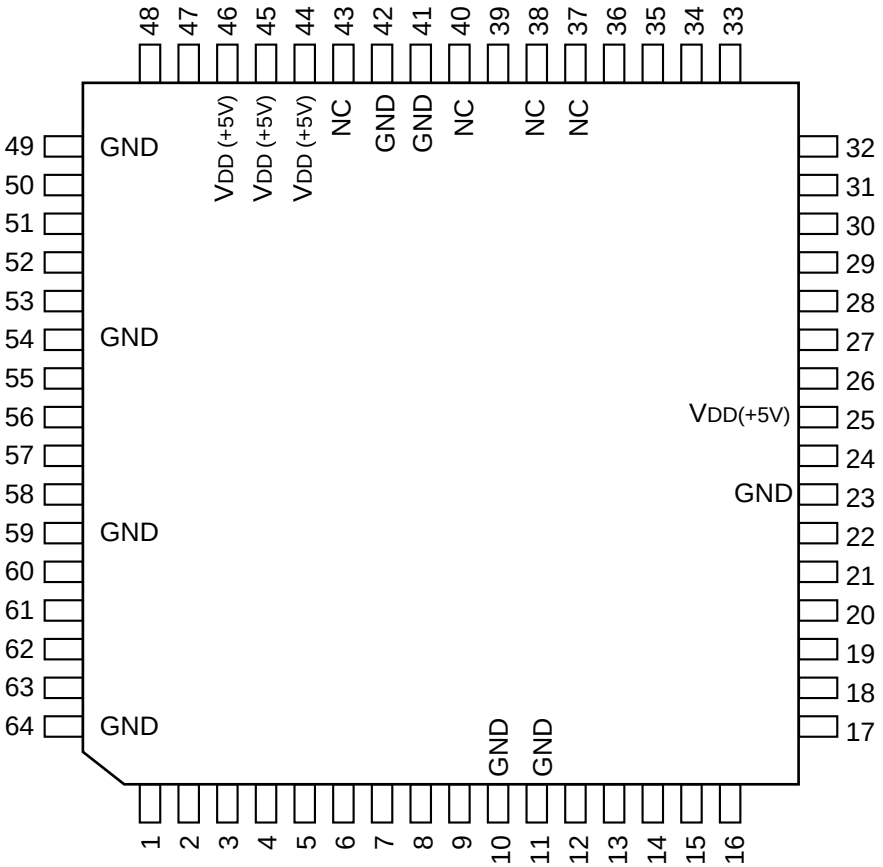
C-MOS FDC (FLOPPY DISK CONTROLLER)

—TOP VIEW—



(VDD = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	8" / $\overline{5"}$	17	I/O	D5	33	I	$\overline{TRK0}$	49	—	GND
2	I	XTALSEL	18	I/O	D6	34	I	$\overline{INDEX}$	50	O	$\overline{STEP}$
3	I	$\overline{RESET}$	19	I/O	D7	35	I	$\overline{RDATA}$	51	O	$\overline{HDIR}$
4	I	E, $\overline{RD}$	20	O	$\overline{DREQ}$	36	I	XTAL2	52	O	$\overline{HLOAD}$
5	I	R/$\overline{W}$, $\overline{WR}$	21	O	$\overline{IRQ}$	37	—	NC	53	O	$\overline{HSEL}$
6	I	$\overline{CS}$	22	I	$\overline{DEND}$	38	—	NC	54	—	GND
7	I	$\overline{DACK}$	23	—	GND	39	I	XTAL1	55	O	$\overline{DS0}$
8	I	RS0	24	O	1/2EX1	40	—	NC	56	O	$\overline{DS1}$
9	I	RS1	25	—	VDD	41	—	GND	57	O	$\overline{DS2}$
10	—	GND	26	I	NUM1	42	—	GND	58	O	$\overline{DS3}$
11	—	GND	27	I	NUM2	43	—	NC	59	—	GND
12	I/O	D0	28	I	IFS	44	—	VDD	60	O	$\overline{MON0}$
13	I/O	D1	29	I	SFORM	45	—	VDD	61	O	$\overline{MON1}$
14	I/O	D2	30	I	$\overline{INP}$	46	—	VDD	62	O	$\overline{MON2}$
15	I/O	D3	31	I	$\overline{READY}$	47	O	$\overline{WGATE}$	63	O	$\overline{MON3}$
16	I/O	D4	32	I	$\overline{WPRT}$	48	O	$\overline{WDATA}$	64	—	GND

INPUT

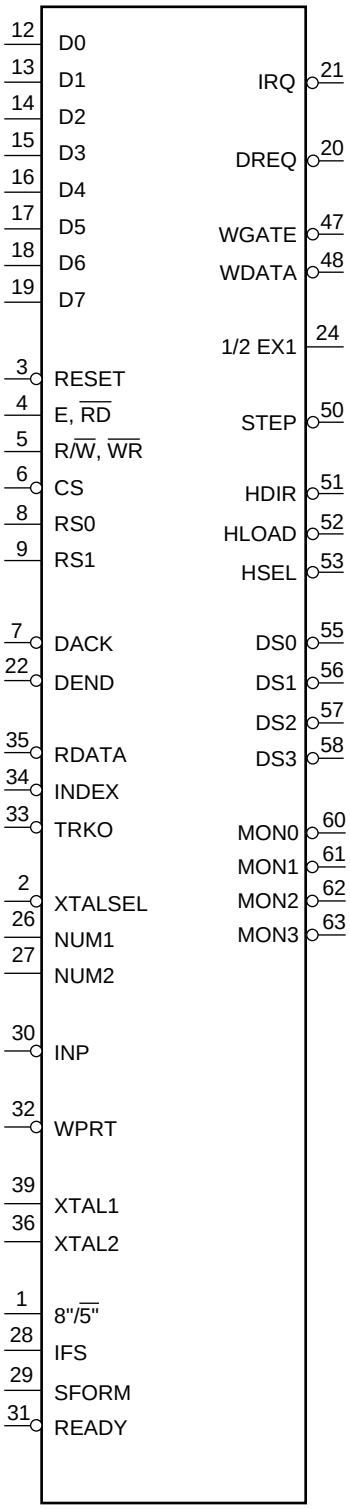
8"/5"	;	DATA TRANSFER RATE SELECT
CS	;	CHIP SELECT
DACK	;	DMA ACKNOWLEDGE
DEND	;	DMA END
E, RD	;	ENABLE, READ
IFS	;	INTERFACE SELECT
INDEX	;	INDEX
INP	;	INPUT PORT
NUM1, 2	;	NOT USER MODE 1, 2
R/W, WR	;	READ/WRITE, WRITE
RDATA	;	READ DATA
READY	;	READY
RESET	;	RESET
RS0, 1	;	REGISTER SELECT 0, 1
SFORM	;	SELECT FORMAT DATA
TRKO	;	TRACK 00
WPRT	;	WRITE PROTECTED
XTAL1, 2	;	XTAL 1, 2
XTALSEL	;	XTAL SELECT

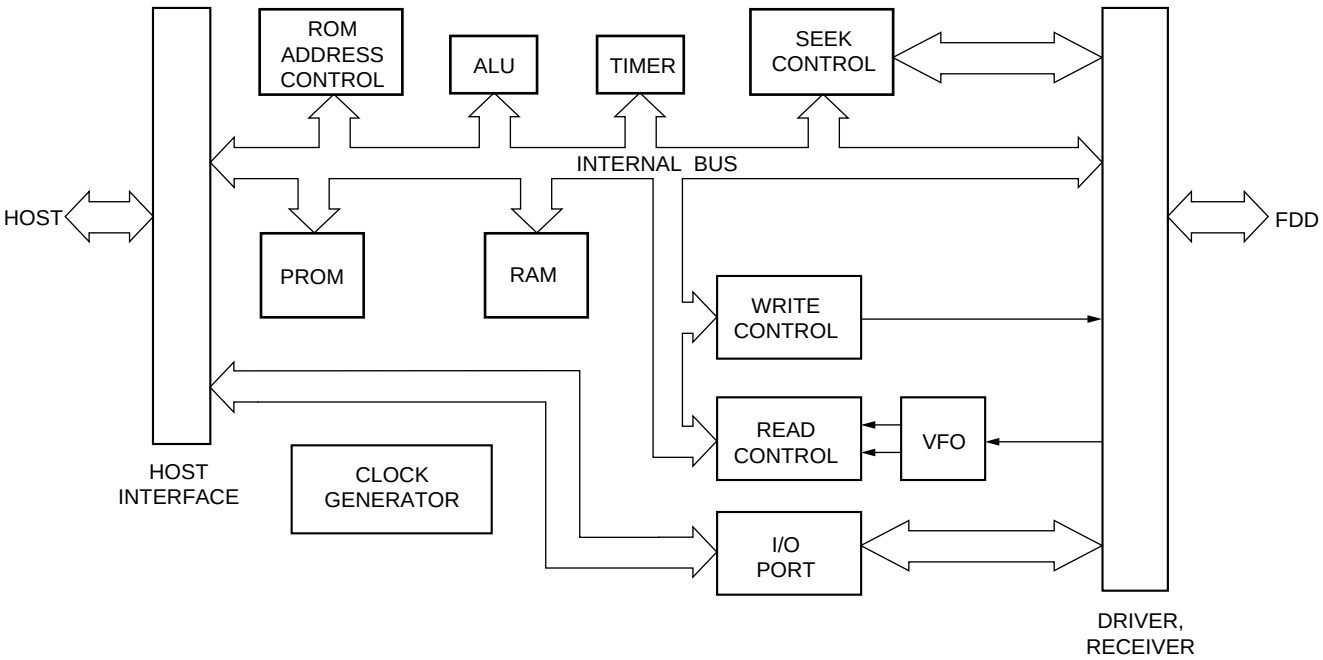
OUTPUT

1/2EX1	;	1/2 EXTAL1
DREQ	;	DMA REQUEST
DS0-DS3	;	DRIVE SELECT 0-3
HDIR	;	HEAD DIRECTION
HLOAD	;	HEAD LOAD
HSEL	;	HEAD SELECT
IRQ	;	INTERRUPT REQUEST
MON0-MON3	;	MOTOR ON 0-3
STEP	;	STEP
WDATA	;	WRITE DATA
WGATE	;	WRITE GATE

INPUT/OUTPUT

D0-D7	;	DATA BUS 0-7





ALU; ARITHMETIC LOGIC UNIT
VFO; VARIABLE FREQUENCY OSCILLATOR