Floppy disk (MFM) data separator design?

11-09-2003, 08:29 PM

Philip Pemberton
Guest
Posts: **n/a**

In message <(E-Mail Removed)>
Mike <(E-Mail Removed)> wrote:

> I'm not sure whether your floppy controller wants to see the encoded data
> (as Jim's PLL data recovery circuit produces) or whether it wants to see
> the recovered data.

Here's an extract from the Rockwell R6765 datasheet (the NEC uPD765 datasheet
says basically the same thing IIRC):

RDD: Read Data.
Read Data input from the floppy disk drive (FDD) containing clock and data
bits.

RDW: Read Data Window.
Data Window input generated by the Phase Locked Loop (PLL) and used to
sample data from the FDD.

VCO: Voltage Controlled Oscillator Sync
This output signal inhibits the VCO in the PLL circuit when low and enables
the VCO in the PLL circuit when high. This inhibits RDD and RDW from being
generated until valid data is detected from the FDD.

> If it expects the data separator circuit to
> decode the data before sending it to the controller, then you'll need to
> add the address mark detector and a divide-by-2 for the clock going to the
> data recovery flip-flop.

I honestly don't know what it expects. The designs I've seen

use an
all-in-one data separator IC, i.e. the SED9420, UM8326, UM8329, FDC9216,
FDC9229 or UM9228.

Thanks.
--
Phil. | Acorn RiscPC600 Mk3, SA202, 64MB, 6GB, (E-Mail Removed) (valid address)| ViewFinder, Ethernet (Acorn AEH62),
http://www.philpem.dsl.pipex.com/ | 8xCD, framegrabber, Teletext
For sale: Minor planetoid. First person to land there gets ownership.

Quote

11-09-2003, 09:21 PM

Mike
Guest
Posts: **n/a**

On Sun, 09 Nov 2003 21:29:14 GMT, Philip Pemberton wrote:

> In message <(E-Mail Removed)>
> Mike <(E-Mail Removed)> wrote:
>
>> I'm not sure whether your floppy controller wants to see the encoded data
>> (as Jim's PLL data recovery circuit produces) or whether it wants to see
>> the recovered data.
> Here's an extract from the Rockwell R6765 datasheet (the NEC uPD765 datasheet
> says basically the same thing IIRC):
> RDD: Read Data.
> Read Data input from the floppy disk drive (FDD) containing clock and data
> bits.

--> That's the key: it's a single line that contains clock and data. It
contains both because it hasn't been decoded.

> RDW: Read Data Window.
> Data Window input generated by the Phase Locked Loop (PLL) and used to
> sample data from the FDD.

--> More on this below.

> VCO: Voltage Controlled Oscillator Sync
> This output signal inhibits the VCO in the PLL circuit when low and enables
> the VCO in the PLL circuit when high. This inhibits RDD and RDW from being
> generated until valid data is detected from the FDD.

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> > all-in-one data separator IC, i.e. the SED9420, UM8326, UM8329, FDC9216,
> > FDC9229 or UM9228.
> >
> > Thanks.

I scrounged up a uPD765 data sheet online, and I'm looking at figure 2,
"System Configuration," on page 5-18 (apparently it came from a databook).
It shows the FDD producing RDD, and a PLL in between the FDD and the uPD765
producing RDW.

Effectively, the floppy output is simply the output of a pulse detector,
which is simply a stream of pulses corresponding to magnetic transitions
(each transition will represent a 1 in the MFM code). That gets fed to the
PLL, which produces the RDW used to clock the data, and also gets fed to
the controller, which uses the RDW input to clock the RDD pulses.

Here's where things get strange. In the Timing Waveforms section, there is
a diagram showing the FDD Read Operation. There, it shows a narrow RDD
pulse in the middle of a half-RDW cycle. That's not the way HDD's ever
worked, but oh well. Jim's system can probably generate the necessary
signals with no problem, although you might have to grab the 'VCO' output
from a different phase of the '164.

What you don't need to do is decode the MFM data, find the address mark, or
anything else. Just send the RDD and RDW to the uPD765, and it should be
happy.

-- Mike --

Quote

11-09-2003, 09:38 PM

Philip Pemberton
Guest
Posts: **n/a**

In message <11pcq639jtm30.990ifztccoko$.(E-Mail Removed)>
Mike <(E-Mail Removed)> wrote:

> I scrounged up a uPD765 data sheet online, and I'm looking at figure 2,
> "System Configuration," on page 5-18 (apparently it came from a databook).

I pulled a copy off Freetradezone (here's a hint - search for "E-Insite
Freetradezone" with google, hit the "I'm Feeling Lucky" button and work from
there). I've been working from Rockwell's R6765/R6265 datasheet. Basically
the same as NEC and SMsC's 765 datasheets, except for a few bits that are
clearer than others (and other bits that are about as clear as mud).

> Here's where things get strange. In the Timing Waveforms section, there is
> a diagram showing the FDD Read Operation. There, it shows a narrow RDD
> pulse in the middle of a half-RDW cycle. That's not the way HDD's ever
> worked, but oh well.

Surely you mean FDDs, not HDDs?

> Jim's system can probably generate the necessary
> signals with no problem, although you might have to grab the 'VCO' output
> from a different phase of the '164.

VCO is an output from the 765 that is used to reset the VCO. I guess I'd
have to add something to clear the shift register when the VCO output on the
765 goes low. An AND gate and an inverter should do it.

> What you don't need to do is decode the MFM data, find the address mark, or
> anything else. Just send the RDD and RDW to the uPD765, and it should be
> happy.

That's good. I can afford to waste (ho hum) a bit of space on the PCB with a
few 74TTL chips. I actually prefer 74TTL for most things except address
decoding. The address decoders I'm using are based on Lattice GALs.

Thanks.
--

Phil. | Acorn RiscPC600 Mk3, SA202, 64MB, 6GB, (E-Mail Removed) (valid address)| ViewFinder, Ethernet (Acorn AEH62), http://www.philpem.dsl.pipex.com/ | 8xCD, framegrabber, Teletext
McBorgs - Over one billion assimilated!

Quote

11-09-2003, 09:58 PM

Uns Lider
Guest
Posts: **n/a**

On 2003-11-09, Philip Pemberton <(E-Mail Removed)> wrote:
> The catch is, most of the ones I've seen use the so-called "Super I/O" chips
> with built-in address decoding. I want a chip I can shove on the bus, add an
> address decoder, then just start sending commands to it.

Hard wire all but the low-order address inputs of the SuperIO to the 0x1f0 or
whatever it's looking for, and hook the read/write strobes to the output of
your external address decoder.

-- uns

Quote

11-09-2003, 10:34 PM

Mike
Guest
Posts: **n/a**

On Sun, 09 Nov 2003 22:38:36 GMT, Philip Pemberton wrote:

> In message <11pcq639jtm30.990ifztccoko$.(E-Mail Removed)>
> Mike <(E-Mail Removed)> wrote:
>
>> I scrounged up a uPD765 data sheet online, and I'm looking at figure 2,
>> "System Configuration," on page 5-18 (apparently it came from a databook).
> I pulled a copy off Freetradezone (here's a hint - search for "E-Insite
> Freetradezone" with google, hit the "I'm Feeling Lucky" button and work from
> there). I've been working from Rockwell's R6765/R6265 datasheet. Basically
> the same as NEC and SMsC's 765 datasheets, except for a few bits that are
> clearer than others (and other bits that are about as clear as mud).
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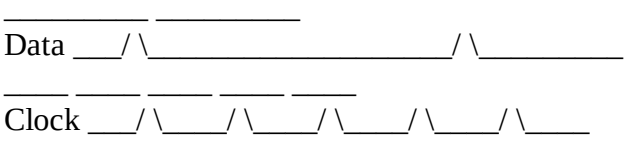
>> a diagram showing the FDD Read Operation. There, it shows a narrow RDD
>> pulse in the middle of a half-RDW cycle. That's not the way HDD's ever

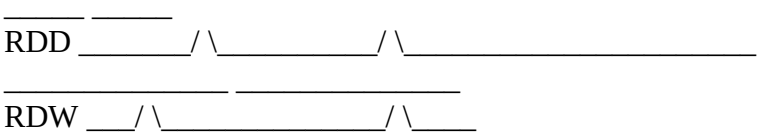
>> worked, but oh well.
> Surely you mean FDDs, not HDDs?

No - I worked mainly on HDDs, which is how I know they worked differently.
Here's the difference:

HDD



FDD (according to the uPD765 data sheet)



In the FDD, RDW really is a window, not a clock. My guess is that they
either have an overclocked sampler in the 765 sampling RDD, or they just
use an SR flip-flop to grab the data, and the next clock edge to reset the
flip-flop.

>> Jim's system can probably generate the necessary
>> signals with no problem, although you might have to grab the 'VCO' output
>> from a different phase of the '164.
> VCO is an output from the 765 that is used to reset the VCO. I guess I'd
> have to add something to clear the shift register when the VCO output on the
> 765 goes low. An AND gate and an inverter should do it.

When I said 'VCO', I meant the '164 in Jim's circuit. It's performing the
function of a VCO is a PLL, even though it's not voltage controlled (and
not even adjustable, except by increasing its length or changing its clock
rate).

In any event, since Jim follows the '164 with a TFF, there probably won't
be glitches at the output, even if you generate glitches when you reset the
'164.

>> What you don't need to do is decode the MFM data, find the address mark, or

>> anything else. Just send the RDD and RDW to the uPD765, and it should be
>> happy.
> That's good. I can afford to waste (ho hum) a bit of space on the PCB with a
> few 74TTL chips. I actually prefer 74TTL for most things except address
> decoding. The address decoders I'm using are based on Lattice GALs.

-- Mike --

Quote

11-09-2003, 10:54 PM

Jim Thompson
Guest
Posts: **n/a**

On Sun, 9 Nov 2003 15:34:08 -0800, Mike <(E-Mail Removed)> wrote:

>On Sun, 09 Nov 2003 22:38:36 GMT, Philip Pemberton wrote:
>
>> In message <11pcq639jtm30.990ifztccoko$.(E-Mail Removed)>
>> Mike <(E-Mail Removed)> wrote:
[snip]
>In the FDD, RDW really is a window, not a clock.

That is correct.

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>either have an overclocked sampler in the 765 sampling RDD, or they just
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>flip-flop.
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>>> signals with no problem, although you might have to grab the 'VCO' output
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>not even adjustable, except by increasing its length or changing its clock
>rate).

It's a PJL (phase-jerked-loop ;-) ...constant frequency but pulled to

correct the phase by the data pulses.

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>be glitches at the output, even if you generate glitches when you reset the
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>> few 74TTL chips. I actually prefer 74TTL for most things except address
>> decoding. The address decoders I'm using are based on Lattice GALs.
>
>-- Mike --

...Jim Thompson
--
James E.Thompson, P.E.	mens
Analog Innovations, Inc.	et
Analog/Mixed-Signal ASIC's and Discrete Systems	manus
Phoenix, Arizona Voice(480)460-2350	
E-mail Address at Website Fax(480)460-2142	Brass Rat
http://www.analog-innovations.com	1962

I love to cook with wine. Sometimes I even put it in the food.

Quote

11-10-2003, 04:08 AM

Michael Black
Guest
Posts: **n/a**

Philip Pemberton ((E-Mail Removed)) writes:
> In message <(E-Mail Removed)>
> "Michael A. Terrell" <(E-Mail Removed)> wrote:
>
>> Fred Abse wrote:
>> > Weren't 5.25" HD disks 300k ? ISTR so.
>> 1.2m on IBM format.
> The formats were, IIRC:
> 3.5" DD - 720k
> 3.5" HD - 1.44MB
> 3.5" QD - 2.88MB
> 5.25" SD - 120k
> 5.25" DD - 360k
> 5.25" HD - 1.2MB
>

> Later.

The problem is that the original line about "300K" was in reference
to the data rate from the drive to the controller. Everything else
is about disk capacity, which is a different thing.

Michael

Quote

11-10-2003, 04:12 AM

Michael Black
Guest
Posts: **n/a**

"Roy J. Tellason" (rtellason@DONTSPAM MEblazenet.net) writes:
> Fred Abse wrote:
>
>> On Sun, 09 Nov 2003 06:29:07 +0000, Philip Pemberton wrote:
>>
>>> In message <(E-Mail Removed)>
>>> Jim Thompson <(E-Mail Removed)> wrote:
>>>
>>>> What is the data rate?
>>> 500 or 250kbits/second. 500kbits if the drive is reading a high density
>>> disk, 250 if it's reading a double-density disk.
>>>
>>> Thanks.
>>
>> Weren't 5.25" HD disks 300k ? ISTR so.
>>
> They were 300 RPM...

Didn't the high density go to 360 RPMs?

Michael

Quote

11-10-2003, 05:32 AM

Mike
Guest
Posts: **n/a**

On Sun, 09 Nov 2003 16:54:40 -0700, Jim Thompson wrote:

>>When I said 'VCO', I meant the '164 in Jim's circuit. It's performing the
>>function of a VCO is a PLL, even though it's not voltage controlled (and
>>not even adjustable, except by increasing its length or changing its clock
>>rate).
>
> It's a PJL (phase-jerked-loop ;-) ...constant frequency but pulled to
> correct the phase by the data pulses.

Sounds like a trademark is in order.

I use the same thing today, but typically with 64 phases instead of 8, and
a loop filter in front of the phase selector. If the jitter from phase
stepping isn't unacceptable, and you can select phases fast enough to track
frequency offsets, it's a great system.

-- Mike --

Quote

11-10-2003, 02:03 PM

Jim Thompson
Guest
Posts: **n/a**

On Sun, 9 Nov 2003 22:32:28 -0800, Mike <(E-Mail Removed)> wrote:

>On Sun, 09 Nov 2003 16:54:40 -0700, Jim Thompson wrote:
>
>>>When I said 'VCO', I meant the '164 in Jim's circuit. It's performing the
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>I use the same thing today, but typically with 64 phases instead of 8, and
>a loop filter in front of the phase selector. If the jitter from phase
>stepping isn't unacceptable, and you can select phases fast enough to track
>frequency offsets, it's a great system.
>
>-- Mike --

Somewhere around here I have a design for a PJL that I did for a
satellite telephone. It features only small jerks allowed plus has
"freewheeling" mode where signal is locked out under noisy conditions.

...Jim Thompson
--
| James E.Thompson, P.E. | mens |
| Analog Innovations, Inc. | et |

| Analog/Mixed-Signal ASIC's and Discrete Systems | manus
|
| Phoenix, Arizona Voice:480)460-2350 | |
| E-mail Address at Website Fax:480)460-2142 | Brass Rat
|
| http://www.analog-innovations.com | 1962 |

I love to cook with wine. Sometimes I even put it in the food.

Quote

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