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Floppy disk (MFM) data separator design?

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                                11-09-2003, 04:43 PM

Goran Larsson
Guest
Posts: **n/a**

In article <(E-Mail Removed)>,
Philip Pemberton <(E-Mail Removed)> wrote:

> The 765 is perfect - it supports the IBM PC formats, it doesn't have a built
> in address decoder and - with a bit of glue logic - will sit on a 6502 CPU's
> bus with very little fuss. The only problem is that wretched data separator.

The 765 is far from perfect. It is popular only because IBM used it in
the original IBM PC. The WD2791, WD2793, WD2795, and WD2797 has internal
data separators for FM and MFM (using a PLL) and can be used with very
little glue logic.

--
Göran Larsson http://www.mitt-eget.com/

Quote

                                11-09-2003, 05:14 PM

Joop
Guest
Posts: **n/a**

Philip Pemberton <(E-Mail Removed)> wrote:

>In message <(E-Mail Removed)>
> "Michael A. Terrell" <(E-Mail Removed)> wrote:
>
>> Is this for a one up, or for production?
>One off.
>
>> If it is a single item, you

>> can still find old IBM PC floppy disk controller cards to salvage the
>> chips you need.
>The catch is, most of the ones I've seen use the so-called "Super I/O" chips
>with built-in address decoding. I want a chip I can shove on the bus, add an
>address decoder, then just start sending commands to it.
>The 765 is perfect - it supports the IBM PC formats, it doesn't have a built
>in address decoder and - with a bit of glue logic - will sit on a 6502 CPU's
>bus with very little fuss. The only problem is that wretched data separator.

I guess you looked at stuff like this already:
"SMSC FDC37C78 Floppy Disk Controller"
http://www.smsc.com/main/catalog/fdc37c78.html

Seems to me that they can be hooked up to a processor similar as I
expect from the 765.

Not sure if they are still available.

Joop

11-09-2003, 05:43 PM

Jim Thompson
Guest
Posts: **n/a**

On Sun, 09 Nov 2003 00:23:48 GMT, Philip Pemberton <(E-Mail Removed)> wrote:

>Hi,
> I'm trying to find a circuit diagram for an MFM data separator suitable for
>connecting to a NEC uPD765, Rockwell R6765 or Intel 8272 FDC. I've found
>loads of ICs capable of doing this, but all the ones I've found were listed
>as obsolete, i.e. no chance of getting a datasheet.
> Has anyone got a circuit that would work with my uPD765? I need this for a
>single-board computer I'm building - replacing the 765 with another IC is not
>an option.
>
>Thanks.

See "FloppyDataExtractor.pdf" on the S.E.D/Schematics page of my
website.

Probably needs some additional logic to mate up to your processor, but

everything about this 20 year old design is standard
off-the-shelf
logic.

...Jim Thompson
--
| James E.Thompson, P.E. | mens |
| Analog Innovations, Inc. | et |
| Analog/Mixed-Signal ASIC's and Discrete Systems | manus
|
| Phoenix, Arizona Voice😕480)460-2350 | |
| E-mail Address at Website Fax😕480)460-2142 | Brass Rat
|
| http://www.analog-innovations.com | 1962 |

I love to cook with wine. Sometimes I even put it in the
food.

11-09-2003, 05:43 PM

Zak
Guest
Posts: **n/a**

Goran Larsson wrote:

> The 765 is far from perfect. It is popular only because
IBM used it in
> the original IBM PC. The WD2791, WD2793, WD2795,
and WD2797 has internal
> data separators for FM and MFM (using a PLL) and can
be used with very
> little glue logic.

The 765 also had the property of not wanting to read if the
track it
thinks it does not correspond with the track IDs coming in.
ISTR the WDs
give you the data (if you want?)

Also the write track (format) command may work
differently.

As for the original question: I'd think the original IBM PCs
may have
used suitable parts, and these must definitely be available at
low cost.

Thomas

11-09-2003, 05:52 PM

Philip Pemberton
Guest
Posts: **n/a**

In message <(E-Mail Removed)>
Joop <(E-Mail Removed)> wrote:

> I guess you looked at stuff like this already:
> "SMSC FDC37C78 Floppy Disk Controller"

> http://www.smsc.com/main/catalog/fdc37c78.html
I've seen that, but I've had no end of trouble locating a sales
rep/distributor in the UK. When I did eventually track down
a distributor,
they decided that I'd need to buy 100 (I kid you not) FDCs
at £19 each (for
a total of £1900), plus postage, plus 17.5% VAT. I think the
total came to
about £2500 - way outside the boundaries of a one-off.

> Seems to me that they can be hooked up to a processor
similar as I
> expect from the 765.
Most of them are software compatible with the 765 as well.
I know how the 765
behaves, what its quirks are and how to tempt it into
behaving itself. I've
done DMA-based data transfers, but not interrupt-based
(non-DMA) data
transfers. In theory, it should just be a case of telling the 765
to grab a
sector, then just pump the data into a RAM buffer. Sure, I'd
have to give the
FDC access to my 6502's NMI pin, but that's not exactly
hard. Interrupt
latency shouldn't be an issue either - the CPU will be
running at 8MHz, maybe
16MHz if I can get it to run that fast.

> Not sure if they are still available.
Depends on your definition of available.

Later.
--
Phil. | Acorn RiscPC600 Mk3, SA202, 64MB, 6GB,
(E-Mail Removed) (valid address)| ViewFinder, Ethernet
(Acorn AEH62),
http://www.philpem.dsl.pipex.com/ | 8xCD, framegrabber,
Teletext
.... I will not steal this tagline, it eez scratched.

[Quote]

11-09-2003, 06:23 PM

Philip Pemberton
Guest
Posts: **n/a**

In message <(E-Mail Removed)>
Jim Thompson <(E-Mail Removed)> wrote:

> See "FloppyDataExtractor.pdf" on the S.E.D/Schematics
page of my
> website.
And "ShiftRegisterPLL.pdf" - same circuit FWICT, except
FloppyDataExtractor
appears to have been done with Protel, ShiftRegisterPLL is
hand-drawn.
Neat design, BTW. Only thing is, the 765 needs to be able to
disable the VCO

on-demand. The VCO pin goes low when the 765 wants to kill the VCO, high to
enable the VCO. I guess I'd need to fit an AND gate and a few inverters into
the line going to the HC164's CLR pin to do that?

> Probably needs some additional logic to mate up to your processor, but
> everything about this 20 year old design is standard off-the-shelf
> logic.
Yum, garden variety TTL. In production for, what, 30 years, yet it still
refuses to die. Brilliant 🙂

Thanks.
--
Phil. | Acorn RiscPC600 Mk3, SA202, 64MB, 6GB,
(E-Mail Removed) (valid address)| ViewFinder, Ethernet (Acorn AEH62),
http://www.philpem.dsl.pipex.com/ | 8xCD, framegrabber, Teletext
Never underestimate the power of human stupidity -- Robert A. Heinlein

[Quote]

11-09-2003, 06:39 PM

Roy J. Tellason
Guest

Posts: **n/a**

Fred Abse wrote:

> On Sun, 09 Nov 2003 06:29:07 +0000, Philip Pemberton wrote:
>
>> In message <(E-Mail Removed)>
>> Jim Thompson <(E-Mail Removed)> wrote:
>>
>>> What is the data rate?
>> 500 or 250kbits/second. 500kbits if the drive is reading a high density
>> disk, 250 if it's reading a double-density disk.
>>
>> Thanks.
>
> Weren't 5.25" HD disks 300k ? ISTR so.
>
They were 300 RPM...

[Quote]

11-09-2003, 06:43 PM

Roy J. Tellason
Guest

Posts: **n/a**

Philip Pemberton wrote:

> In message <(E-Mail Removed)>
> "Michael A. Terrell" <(E-Mail Removed)> wrote:
>
>> Fred Abse wrote:
>> > Weren't 5.25" HD disks 300k ? ISTR so.

>> 1.2m on IBM format.
> The formats were, IIRC:
> 3.5" DD - 720k
> 3.5" HD - 1.44MB
> 3.5" QD - 2.88MB
> 5.25" SD - 120k

That one should be 180k.

> 5.25" DD - 360k
> 5.25" HD - 1.2MB
>
> Later.

And these only hold for "IBM" formats. Kaypro, for one example, would store
390K on a "360k" floppy. My Osborne Executive would store 183K on a SSDD
disk.

Quote

11-09-2003, 07:15 PM

Jim Thompson
Guest
Posts: **n/a**

On Sun, 09 Nov 2003 19:23:42 GMT, Philip Pemberton <(E-Mail Removed)> wrote:

>In message <(E-Mail Removed)>
> Jim Thompson <(E-Mail Removed)> wrote:
>
>> See "FloppyDataExtractor.pdf" on the S.E.D/Schematics page of my
>> website.
>And "ShiftRegisterPLL.pdf" - same circuit FWICT,

Yep, I forgot I had already posted the hand-drawn version ;-)

>except FloppyDataExtractor
>appears to have been done with Protel,

An old, old version of OrCAD before the Windows munge.

>ShiftRegisterPLL is hand-drawn.
>Neat design, BTW. Only thing is, the 765 needs to be able to disable the VCO
>on-demand. The VCO pin goes low when the 765 wants to kill the VCO, high to
>enable the VCO. I guess I'd need to fit an AND gate and a few inverters into
>the line going to the HC164's CLR pin to do that?

Depends on what "kill the VCO" means?

>
>> Probably needs some additional logic to mate up to your processor, but

>> everything about this 20 year old design is standard off-the-shelf
>> logic.
>Yum, garden variety TTL. In production for, what, 30 years, yet it still
>refuses to die. Brilliant 🙂
>
>Thanks.

Funny how I am... though I'm a custom chip designer I avoid custom
chips like the plague when I'm doing G-jobs. Then, if I need them 20
years later, there's no problem replicating them ;-)

...Jim Thompson
--
James E.Thompson, P.E.	mens
Analog Innovations, Inc.	et
Analog/Mixed-Signal ASIC's and Discrete Systems	manus
Phoenix, Arizona Voice😦480)460-2350	
E-mail Address at Website Fax😦480)460-2142	Brass Rat
http://www.analog-innovations.com	1962

I love to cook with wine. Sometimes I even put it in the food.

11-09-2003, 07:41 PM

Mike
Guest
Posts: **n/a**

On Sun, 09 Nov 2003 15:04:31 GMT, Philip Pemberton wrote:

> In message <(E-Mail Removed) t>
> Fred Abse <(E-Mail Removed)> wrote:
>
>>> 500 or 250kbits/second. 500kbits if the drive is reading a high density
>>> disk, 250 if it's reading a double-density disk.
>> Weren't 5.25" HD disks 300k ? ISTR so.
> In FM mode, yes, IIRC. I'm using 3.5" HD disks which are usually recorded at
> 500k/sec in MFM mode with a spindle speed of (IIRC) 360rpm.
> The problem is, without a data separator, the controller ICs are useless. FM
> isn't too hard - I've got a schematic for that. MFM encoding, OTOH, is a
> total PIB. I spent most of this morning searching through Google and the
> EspaceNet patent information system. And what did I find? Nothing useful :-(
>
> Thanks.

The MFM code is relatively painless to implement (more on that shortly). If
you're looking for patents, I have a proprietary paper from some years ago
that discusses myriad modulation codes, MFM among them, and points out that
until the mid-70's, MFM was used in all IBM disk and Ampex tape drives. The
origins of the code are disputed; the author provides three references:

1. W.H.P. Pouliart, J.P.H. Vandevenne, "Electrical Intelligent Storage
Arrangement," US Patent 2,807,004, issued Sept 17, 1957

2. Armin, Miller, "Recording and/or Reproducing System," US Patent
3,108,261, issued Oct 28, 1963 (Ampex).

3. G.V. Jacoby, "Magnetic Recording and Reproducing of Digital
Information," US Patent 3,414,894, issued Dec 3, 1968 (RCA).

Now, back to the code. The MFM encoding table is simply:

Data Code
0 B0
1 01

Since two code bits are written for each data bit, the code rate is twice
the data rate. The B in the B0 code means "the inverse of the previous code
bit." A moment's study will reveal that if the previous data bit was a 0,
the previous code bit was also 0, so the first code bit is 1. Similarly, if
the previous data bit was 1, the first code bit is 0.

Also, note that the encoded data consists of a meaningless bit followed by
the data bit. To decode MFM, simply save every other bit - but make sure
you get the right "other" bit.

The missing information is how to synchronize to the data pattern so you
get the right bit. At the start of each sector, there's a preamble, which
is a simple repeating pattern that the PLL uses to acquire timing. After

that, there's an address mark, which is a fixed pattern that's different
than the preamble. The preamble and address mark are the same for every
sector on the disk. Following the address mark is the data - a fixed number
of bytes. Following the data are one or two CRC bytes to check for data
corruption.

I'm not sure whether your floppy controller wants to see the encoded data
(as Jim's PLL data recovery circuit produces) or whether it wants to see
the recovered data. If it takes the encoded data, then you don't need any
of the information above. If it expects the data separator circuit to
decode the data before sending it to the controller, then you'll need to
add the address mark detector and a divide-by-2 for the clock going to the
data recovery flip-flop. The controller probably handled the error
correction testing, so you don't need to worry about that.

Last, it would be best to implement a clock-stopping scheme that prevents
glitches on the RCLK line. Controllers are often quite finicky about their
clocks, and are prone to making mistakes when they see glitches.

-- Mike --

Quote

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