Designing with the DP8461

National Semiconductor
Application Note 415
Kern Wong
April 1985

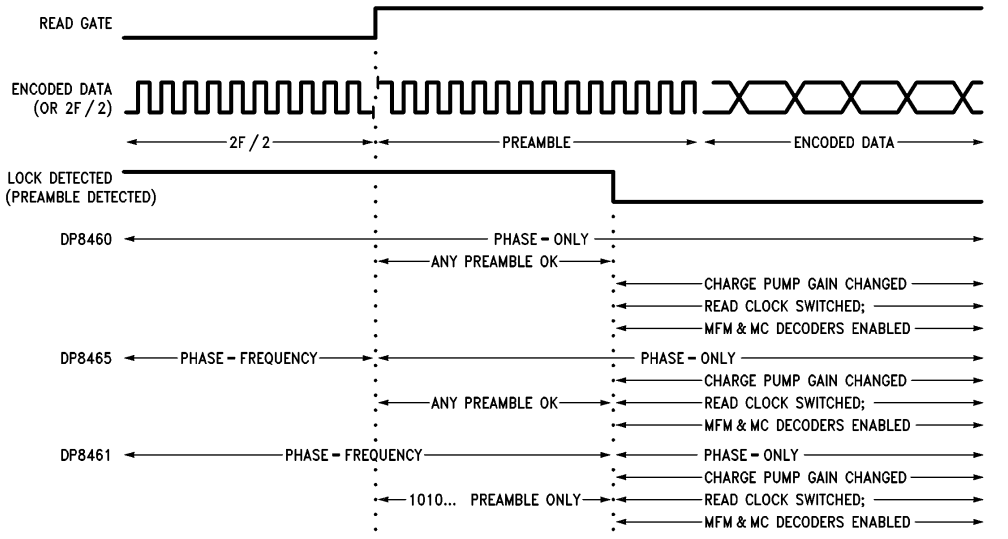
GENERAL DESCRIPTION

The DP8461 is one of the second generation data separator/synchronizer products introduced following the highly successful DP8460 single chip PLL circuit for applications in rotational memory storage systems. The DP8461 consists of the same basic functional blocks as the first generation device (DP8460). It has a proprietary pulse-gate which features an accurate silicon delay line, an edge-triggered digital phase comparator, a high speed matched charge pump, high impedance buffer amplifier, and a temperature compensated stable voltage-controlled-oscillator (VCO). It also contains MFM decoder, missing clock detector, and lock-detect control circuitry for maximum design flexibility.

Like the DP8465, the DP8461 performs PHASE-FREQUENCY COMPARISONS in the non-read mode (READ GATE is ''Low''). This enhancement eliminates the possibility of false lock to the reference signal during a power-up sequence or when returning from a read operation. Furthermore, the DP8461 has been designed to allow PHASE-FREQUENCY COMPARISONS to continue into the preamble field during read mode (READ GATE is ''High''). This feature eliminates the possibility of a Quadrature Lock or Harmonic Lock problem occurring in the PLL synchronization field. In order to take advantage of phase-frequency comparison during preamble detection, the DP8461 requires a ''Qualified Read-Gate'' (that is the READ GATE shall be asserted only within the preamble or maximum frequency field span). Since the DP8461 looks for a 1010. . . encoded data pattern while doing PHASE and FREQUENCY COMPARISONS in the read mode, it must be used only with a code employing this preamble such as MFM, (1,7) or (1,8). The DP8461 is pin-for-pin compatible with the DP8460 and DP8465 parts; and is also functionally equivalent to them with the exceptions of extended Phase-Frequency Comparison during preamble and a ''Qualified Read-Gate'' requirement. The DP8461 can be used as a synchronizer for MFM, (1,7), and (1,8) codes or as a data separator for MFM only. *Figure 1* shows a diagrammatic comparison of the key functional features of the three part types mentioned above.

CIRCUIT OPERATION

The DP8461 is in the non-read mode whenever the READ GATE is deasserted (Low). The 2F REFERENCE CLOCK INPUT is divided by two and transmitted to the READ CLOCK OUTPUT via a multiplexer. In this mode the VCO DIVIDED BY TWO is locked onto the 2F CLOCK DIVIDED BY TWO, keeping the VCO close to the data frequency in anticipation of locking onto the actual data stream. While in the non-read mode, PHASE-FREQUENCY COMPARISONS are always employed to eliminate any possibility of false lock.



TL/F/8599–1

FIGURE 1. DP8460/65/61 Modes of Operation Comparison Diagram

RRD-B30M105/Printed in U. S. A.

Since the DP8461 continues to make PHASE-FREQUENCY COMPARISONS when the read mode is entered, the assertion of READ GATE should only occur over a PREAMBLE or 1010. . . pattern. The DP8461 enters the read mode after a selectable delay time which may be either one or thirty-two VCO cycles. The 2-byte (32 VCO cycles) delay is useful in hard-sectored drives for allowing a gap pattern to pass before the PLL locks onto the data pattern. Soft-sectored drives do not need this delay. Once in the read mode, the PLL reference input is switched from the 2F CLOCK source to the ENCODED DATA INPUT. The PLL remains in the high track rate mode and continues to perform PHASE-FREQUENCY COMPARISONS to quickly lock onto the repetitive encoded preamble.

By careful selection of the loop filter components, it takes less than one byte time for the VCO to lock onto the data stream sufficiently for preamble detection to begin. As soon as 2 bytes (16 consecutive pulses) of the selected (ones or zeroes pattern) preamble are detected, the $\overline{\text{LOCK DETECTED}}$ OUTPUT goes low and this causes the PLL circuit to switch from PHASE-FREQUENCY comparisons to PHASE-ONLY comparisons. In a typical disk drive application, the $\overline{\text{LOCK DETECTED}}$ OUTPUT may be directly connected to the $\overline{\text{SET PLL LOCK INPUT}}$. When a low level is present on the $\overline{\text{SET PLL LOCK INPUT}}$, the CHARGE PUMP changes from a high to low tracking rate, the source of the READ CLOCK signal switches from the 2F CLOCK INPUT to the VCO CLOCK, and the MFM decoder becomes enabled and begins to output decoded NRZ data. If the DP8461 is employed as a data separator for MFM encoded data, the READ CLOCK OUTPUT and the NRZ READ DATA OUTPUT (which is synchronized to the READ CLOCK) should be used. These TTL compatible signals can be connected directly to a Disk Data Controller such as the DP8466 which controls Winchester or floppy disk drives. The MISSING CLOCK DETECTED OUTPUT can also be utilized for MFM-encoded data for soft-sectored disk drives. It should be noted, however, the circuit is designed only to recognize a missing MFM clock-bit which is framed by two existing clock bits. In order to insure the detection of an address mark, simultaneous monitoring of the NRZ output for an ''A1'' hexidecimal code and the MISSING CLOCK DETECTED OUTPUT for a single pulse within the same byte time is necessary.

When the READ GATE goes low, signifying the end of a read operation, the PLL reference signal is switched back to the 2F CLOCK and the $\overline{\text{LOCK DETECTED}}$ OUTPUT goes high, causing the VCO gating circuitry within the PULSE GATE to be bypassed thus allowing PHASE and FREQUENCY comparisons to occur. The PLL also returns to the high tracking rate and the output signals return to their initial conditions.

If the chip is used as a data-synchronizer (on-chip decoding not necessary) for MFM or other popular RLL codes employing a 1010. . . preamble, the SYNCHRONIZED DATA OUTPUT and the VCO CLOCK OUTPUT should be used. External decoding can be accomplished either in commercially available controller chips or encoder/decoder circuits, or by the customer's proprietary design.

PHASE ONLY VS. PHASE-FREQUENCY COMPARISON OPERATION

As stated earlier, the function of the PLL is to maintain phase and frequency lock between the reference signal (2F CLOCK or ENCODED DATA) and the feedback signal (VCO). A comparator that performs only phase comparison is mandatory during read-mode in the data field in order to handle the non-periodic nature of various coding schemes. With this type of detector, the phase-locked-loop functions as a feedback loop in which it responds only to the phase differences between the input and the feedback waveforms. As long as the reference and VCO singals have their edges aligned (are in phase lock), the PLL is insensitive to their frequency relationship.

During the non-read mode the PLL is required to lock onto the 2F CLOCK, a specific frequency reference that is close to the data rate. If a disturbance is somehow introduced in the system which results in cycle slipping or prolonged transient behavior of the reference clock, false lock may occur if a PHASE-ONLY comparator is being used. Similarly, in the preamble field during read mode, the PLL tries to lock onto a periodic pattern. If pulse-pairing occurs in this PLL synchronization field due to asymmetry in disk drive electronics, quadrature lock may result if a PHASE-ONLY comparator is being used. Under these circumstances PHASE comparison alone may be inadequate, since it discriminates only phase and not frequency information. A PHASE-FREQUENCY-COMPARATOR, therefore, is recommended during these modes of operation whenever false lock presents a potential problem. The DP8461 implements such a comparator. It performs identically to the PHASE-COMPARATOR in the case when both inputs to the comparator have the same frequency; however, if the inputs exhibit the slightest frequency offset, the PHASE-FREQUENCY-COMPARATOR also provides a frequency-sensitive error correction signal to ensure frequency acquisition.

As mentioned in the device description, the DP8461 requires a ''Qualified Read-Gate'' for proper operation in soft-sectored environments. This is necessary to accommodate phase-frequency comparison into the preamble field. If the READ GATE is allowed to be asserted randomly, it might be asserted in the data field or in the write-splice area. With the DP8461, prior to preamble detected, the PLL is operating in the phase-frequency mode. If it encounters a low frequency pattern in the data field, the VCO will try to lock onto it and thus shift its frequency. Similarly, if READ GATE becomes active in a write-splice area, the PLL may be pushed to either of its limiting frequency excursions. By employing a ''Qualified Read-Gate'' with the DP8461, the READ GATE will always be asserted over a repetitive 1010. . . pattern and thus avoid any of these problems.

PULSE GATE

The PULSE GATE has two important functions. It ensures a continuous PLL lock in the presence of random patterns encountered on the media and in the bit stream. It also provides a precise time delay (independent of process and

external component variations) necessary to align the incoming data with the center of the decoding window. The delay is exactly one-half the period of the 2F CLOCK and the delay generator is referenced to the 2F CLOCK. This allows input bit jitter up to ±one-half the 2F CLOCK period.

The PULSE GATE incorporated in the DP8461 has two multiplexers which allow the circuit to switch from PHASE-FREQUENCY COMPARISON to PHASE-ONLY COMPARISON when the LOCK DETECTED signal becomes active (Low). *Figure 2* is a block diagram of the PULSE GATE which details how this is accomplished. When both the INTERNAL READ GATE and the INTERNAL LOCK DETECTED are inactive (non-read mode) the 2F CLOCK DIVIDED BY TWO and the VCO DIVIDED BY TWO signals are selected by MULTIPLEXER-1 and MULTIPLEXER-2 respectively. In this configuration phase and frequency comparisons are made between them and the possibility for a false lock occurrence is eliminated. When the INTERNAL READ GATE is active while the INTERNAL LOCK DETECTED remains inactive (read-mode, preamble detection) the ENCODED DATA and the VCO DIVIDED BY TWO signals are selected by the multiplexers. Again, PHASE-FREQUENCY COMPARISONS continue to be performed to ensure the PLL locks exactly to the data rate frequency. After sixteen pulses of consecutive preamble pattern are detected, the INTERNAL LOCK DETECTED line becomes active. MULTIPLEXER-2, under the control of the INTERNAL LOCK DETECTED singal, then switches from the VCO DIVIDED BY TWO to the GATED VCO signal. Through the circuit configured by the D-type flip-flops and the OR gate, the comparator effectively performs PHASE-ONLY comparisons (an INTERNAL VCO pulse is allowed to the input of MUX-2 only when an ENCODED DATA pulse is sensed). Thus, the DP8461 guarantees proper frequency lock of the VCO to the 2F REFERENCE CLOCK during the non-read mode and to the preamble synchronization pattern during the read mode. The circuit performs the necessary phase-only comparison in the data field during read mode operation.

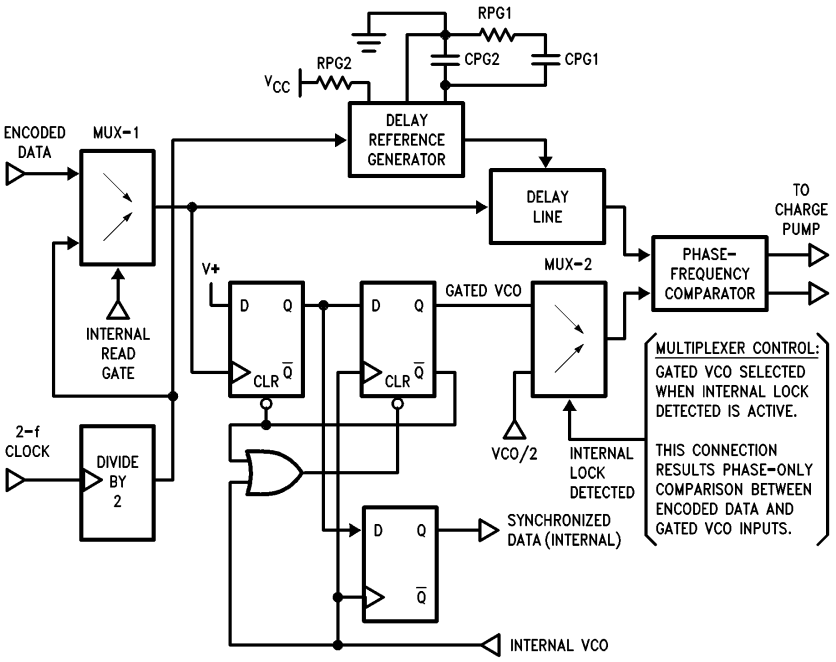
DATA SEPARATOR APPLICATION PROBLEMS

Following are some common application problems for many data separator circuit designs. The purpose of this application note is to identify these problems and to propose simple solutions thus enabling our DP8461 users to avoid these potential application problems.

FORMS OF FALSE LOCK

Two types of pseudo-lock can typically occur in a PLL within a disk drive system. A periodic input waveform must be present, such as a disk synchronization field, in conjunction with the suppression of frequency information (pulse-gate type PLL) in order for either to occur.

Pulse Gate Block Diagram



TL/F/8599–2

FIGURE 2

I. The first is herein termed simply ''false lock'', or more accurately, **fractional harmonic** lock. This occurs when the PLL is disturbed, forcing the VCO outside of the capture range (determined by the loop bandwidth; typically ±2% of the data rate) of the PLL for a period of time. The PLL is then able to acheive a pseudo-lock if (1) the ratio of the VCO frequency vs. the input frequency is an integer fraction, such as 5:6 or 6:5, and (2) the difference frequency between the VCO and the input is greater than the PLL capture range. Ideally, the error signal generated at the VCO control input, which is at the ''beat'' (difference) frequency of the two signals, would correct the false lock. However, this error signal is suppressed because it lies outside the frequency range of the low pass loop filter. The loop will, however, produce a self-sustaining error signal and thus will remain on the false lock null.

II. The second form of pseudo-lock is called **quadrature lock**. In this case, the PLL is able to lock to the correct frequency, but is caught on a narrow phase null which is positioned 90 degrees (w. r. t. the NRZ data period) from nominal. This phase null can occur only when there exists a pairing of periodic disk data pulses which originates in the disk drive itself (see *Figure 3*). The quadrature lock is perpetuated because the net error signal generated at the VCO input by the displaced, complimentary pulses lies well outside of the loop bandwidth and is averaged to a self-sustaining correction signal.

LOSS OF LOCK DURING READ MODE

In some systems the controller asserts the READ GATE randomly along a formatted track. If the READ GATE is asserted over a write splice, which usually contains unintelligible information, the PLL might false lock to some harmonic of the data or it might be pushed to either extreme of its allowed frequency swing. Similarly, when the READ GATE is asserted over a data field the PLL might lock to a harmonic of the data.

This problem can be completely avoided with the DP8461, which is used in conjunction with a ''Qualified Read-Gate'' technique. As an example, a good PLL controller algorithm that only allows assertion of the READ GATE over a preamble or similar high frequency pattern is listed below.

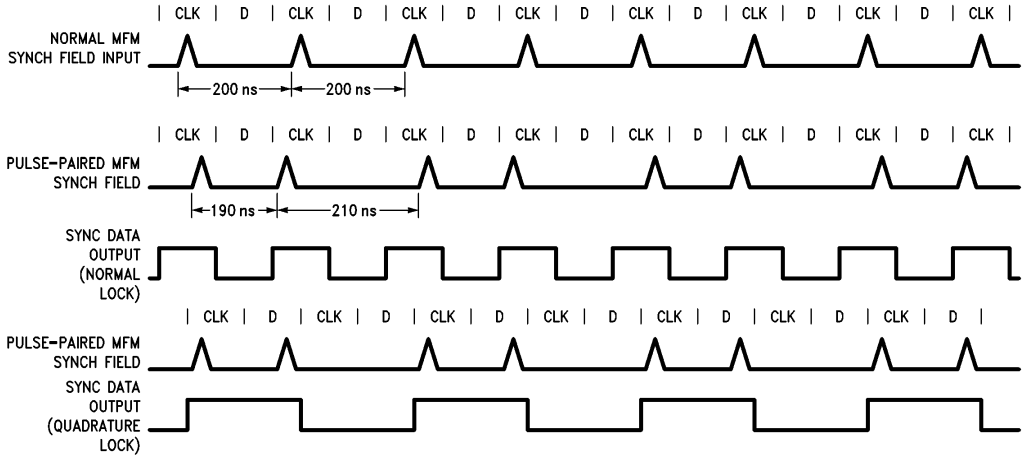
1) Deassert READ GATE—allow a 4 byte time minimum for the PLL to lock to the 2F-REFERENCE CLOCK.
2) Wait for 2.5 bytes of valid preamble pattern.
3) Assert READ GATE.
4) If valid preamble continues for 5 or more bytes then go to 5; otherwise go to 1.
5) ''LOCK DETECTED'' becomes active, AM search begins.
6) If AM is found, then continue the read routine; otherwise go to 1.

FALSE LOCK IN THE NON-READ MODE

The DP8461 **has been specifically designed to eliminate the possibility of false lock during the non-read mode**. This is accomplished by the use of a phase-frequency comparator in the non-read mode as was described in the PULSE GATE section.

False lock during the non-read mode can occur by two means in systems using phase-only comparisons in the non-read mode. When the power supply of the PLL circuit is switched on for the first time, the VCO ramps toward the reference frequency. The acquisition process may lock the VCO to some harmonic of the 2F REFERENCE CLOCK if the bandwidth (capture range) is not high enough. False lock can also occur in the non-read mode after an aborted read operation as described above. If the VCO has either lost lock or has been driven far from its center frequency while trying to read, false lock might occur during relock to the crystal if the capture range is narrow.

Example shows 5 Mbit/sec MFM synchronization field.
Input data bit positions are indicated by peaks of pulses.



TL/F/8599–3

FIGURE 3. Timing Diagram of PLL Quadrature Lock within a Symetrically Pulse-Paired Synch Field

QUADRATURE LOCK

The DP8461 **has been specifically designed to eliminate the possibility of both quadrature lock and harmonic lock in the preamble field during read mode** by extending the phase-frequency comparison technique during preamble detection in the read mode until LOCK DETECTED occurs.

Within the standard synchronization field which precedes the data field, bits are recorded at a constant frequency for a time sufficient to allow the PLL to acquire lock. With normal recording and read-circuit behavior, this synchronization information reaches the PLL as a continuous, periodic data stream. In some disk drives, if an offset has somehow been induced into the recorded information, or if read-channel asymmetry exists within the drive electronics which skews the flux reversal zero-crossing point, the synchronization field waveform which reaches the PLL may appear in the form of periodic pulse-pairs. This condition only arises when a repetitive pattern is present, giving rise to the possibility of quadrature lock. Note that quadrature lock is actually more prone to occur within systems where a low-noise design has minimized the randomizing effect which noise has on bit position.

MINIMUM PULSE WIDTH REQUIREMENT

The DP8461, as with other members of the DP8460 family of data synchronizers, has a minimum pulse width requirement on the ENCODED DATA input for proper operation. As there is no uniform pulse width specification on ''Raw Read Data'' outputs from disk and tape drive manufacturers, it has been found that certain drive systems output too narrow a pulse width for the DP8460 family of circuits to accept. Our recommended minimum positive pulse width is 6 ns and the minimum negative pulse width is 80% of the VCO period; this allows a maximum positive pulse width of 120% of the VCO period. Some drives utilize a bidirectional one-shot to shape the read data output pulse. The output pulse width from such drives can be readily readjusted from an RC timing network to attain acceptable minimum pulse width requirements for the PLL circuits.

Note: The chip is particularly sensitive to inadequately filtered switching supply noise.

SUMMARY

The DP8461 is another one of National's second generation single chip high performance PLL circuits for application in disk memory systems. This device features a comparator with both phase-frequency and phase-only comparison capabilities. Additionally, the PHASE-FREQUENCY COMPARISON circuit in the DP8461 has been designed to allow its operation in the preamble field during read mode so that employing it with a ''Qualified Read-Gate'' will eliminate all potential false and quadrature lock problems associated with soft-sectored systems. The DP8461 offers significant savings of cost and time in production, test, and maintenance since only a few fixed passive components are required for operation. The need to trim any external components has been eliminated and, since no external components determine window accuracy, the performance will not be sensitive to external variations. The chip requires a single +5 volt supply and it is housed in a narrow 24-pin dual-in-line package (also available in 28 pin PCC package). The DP8461 has the same pinout as the DP8460 and the DP8465, and thus, can be used in their designed applications provided the READ GATE has been qualified. The DP8461 can be used as a data synchronizer for MFM or any of the existing RLL codes employing a 1010. . . preamble, or as a data separator for MFM.

For further information, the reader should also refer to the National Semiconductor Application Note 414, Precautions for Disk Data Separator (PLL) Designs.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408